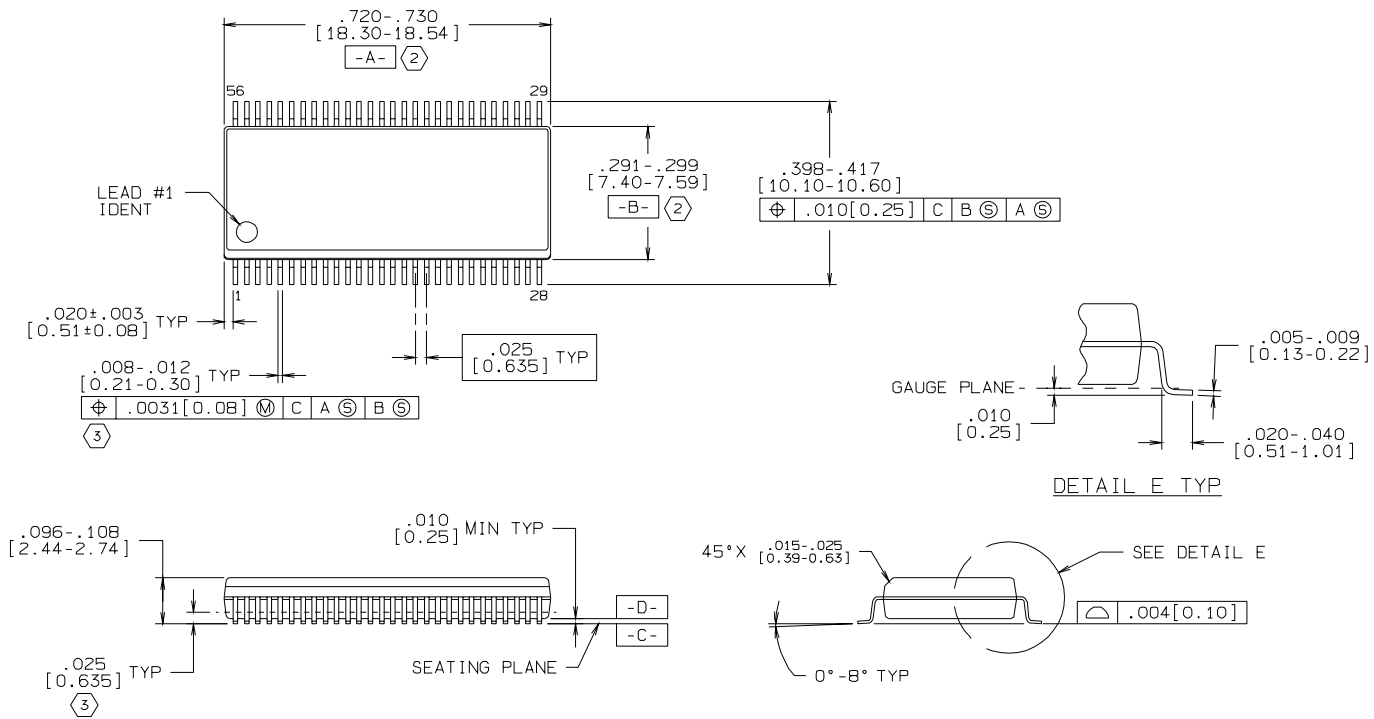


REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	08421	03/28/91	KES/CC
B	POSITION TOL .007[0.18] WAS .010[0.25]; ADD NOTE 4.	10178	03/30/94	DEG/CC
C	TRUE PDS: .0063[0.16] WAS .007[0.18]; LD PITCH: [0.635] WAS [0.63]; STANDOFF: .010[0.25] MIN WAS .008-.016 [0.21-0.40]; LD TIP TO LD TIP: .398-.417[10.11-10.59] WAS .395-.420[10.04-10.66].	10494	07/19/94	MS/DM
D	ϕ .0031[0.08] ϕ C A ϕ B ϕ WAS ϕ .0063[0.160] ϕ D A ϕ B ϕ	10605	09/26/94	MS/KHT
E	TOP VIEW; ADD DIM .020 \pm .003[0.51 \pm 0.08]; CHANGE DWG SIZE FROM B TO C.	11230	11/01/95	MS/



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED

- STANDARD LEAD FINISH:
200 MICROINCHES/5.08 MICROMETERS MINIMUM LEAD/TIN
(SOLDER) ON COPPER.
- DIMENSION DOES NOT INCLUDE MOLD FLASH.
- MAXIMUM LEAD WIDTH ABOVE AREA SPECIFIED .018[0.45].
- REFERENCE JEDEC REGISTRATION MO-118, VARIATION AB, DATED JUNE 1993.

APPROVALS	DATE	National Semiconductor 2900 Semiconductor dr, Santa Clara, CA 95052-8090			
DRAWN <i>Rut Sturcken</i>	03/28/91	MOLDED PACKAGE, SSOP, .300 WIDE, 56 LEAD			
DFTG. CHK.					
ENGR. CHK.					
PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]		N/A	C	MKT-MS56A	E
DO NOT SCALE DRAWING			SHEET 1 OF 1		