CF+ and CompactFlash Specification Revision 1.4

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1 General

1.1 Introduction

The CompactFlash Association (CFA) was established in October 1995 with the premise that CompactFlash (CF) technology would enable the introduction of a new class of advanced, small lightweight, low power mobile products that would significantly increase the productivity and enhance the lifestyles of millions of people.

The concept behind CF technology was simple: to capture, retain and transport data, audio and images on CompactFlash Storage Cards. CF Storage Cards provided the capability to easily transfer all types of digital information and software between a large variety of digital systems. The CFA approved and published the CompactFlash standard. This vendor-independent specification enabled users to develop CF products that function correctly and are compatible with future CF designs, eliminating compatibility issues.

Now the CFA has developed the CF+ specification to expand the CF concept beyond flash data storage and include I/O devices and magnetic disk data storage. The CF+ specification also includes the original Type I (3.3mm thick) card and newer Type II (5mm thick) cards. While CompactFlash and many I/O devices can fit into the Type I card, the Type II cards enable higher capacity CompactFlash cards, magnetic disk cards and many additional I/O cards.

1.2 CFA Goals and Objectives

The goals of the CFA are to promote and encourage the worldwide adoption of CF+ and CompactFlash (CF) technology as an open standard. The association's primary objectives are to drive second-source availability; to promote acceptance of the CF+ specification as an industry standard across platforms and markets internationally; to ensure compatibility for users of CF and CF+ products, and to evolve the approved CF+ standard over time while ensuring backward compatibility.

1.3 Overview of CompactFlash Storage Card

CF+ is a small form factor card standard that encompasses CompactFlash (CF) flash data storage cards, magnetic disk cards and I/O cards including, but not limited to serial cards, Ethernet cards, fax/modem cards and wireless pager cards.

The CF+ card provides high capacity data storage and I/O functions that electrically comply with the Personal Computer Memory Card International Association standard. (In Japan, the applicable standards group is JEIDA.) Minor differences between the CF+ Specification and the PC Card ATA standard are documented in the Appendix at the end of this specification. Although the size of a matchbook, CF+ and CompactFlash Cards can be used with passive adapters in a PC-Card Type II or Type III socket.

A CompactFlash Storage Card also runs in True IDE Mode that is electrically compatible with an IDE disk drive. Other CF+ devices such as magnetic disk drives may also run in True IDE Mode.

The CompactFlash Storage Cards on-card intelligent controller manages interface protocols, data storage and retrieval as well as Error Correcting Code (ECC), defect handling and diagnostics, power management and clock control. Once the CompactFlash Storage Card has been configured by the host, it appears to the host as a standard ATA (IDE) disk drive.

Similar controller functions are used with other CF+ cards allowing a wide variety of devices to be compatible with the CF+ specification

1.4 Related Documentation

- PCMCIA PC Card Standard, 1995
- PCMCIA PC Card ATA Specification, 1995

  These documents can be obtained from: PCMCIA
  2635 North First St., Ste. 209
  San Jose, CA 95131 USA
  Phone: 408-433-2273
  Fax: 408-433-9558

- AT Attachment Interface Document, American National Standards Institute, X3.221-1994

  This document can be obtained by calling Global Engineering Documents at 1-800-854-7179.

1.5 Compatibility Requirements

CompactFlash and CF+ are trademarks of the CompactFlash Association. All products that conform to this specification may use the CompactFlash and CF+ names with the appropriate license from the CompactFlash Association.

The goal of this specification is to conform to the PC Card Specification when operating in the PCMCIA mode and to conform to the ATA specification when operating in the True IDE Mode. If there is a conflict between this specification and the PC Card or the ATA Specifications, the CompactFlash Specification will apply.

To conform to this specification, a CompactFlash Storage Card or CF+ Card must conform to all physical, electrical and Metaformat specifications in this document. A CompactFlash Storage Card must implement all PC Card and True IDE ATA commands listed in this specification. Commands can be implemented as “no operation” to meet this requirement. In addition, a CompactFlash card must implement all commands in section 6 except the Security commands (F1 to F6). While the security commands are optional, CFA members are encouraged to implement them.

2 Scope

2.1 Elements of this Specification

This specification is divided into five sections: Card Physical, Electrical Interface, Metaformat, Software Interface and CompactFlash Adapter. A brief overview of each section follows.

2.2 Card Physical

This section defines the dimensions and mechanical tolerances for CompactFlash Storage Cards and CF+ Cards. Specific pin lengths are defined to ensure that power is applied first and removed last during card insertion and removal. Reliability factors, such as connector mate/unmate cycles, environmental operating conditions and test methods are also specified.

2.3 Electrical Interface

This section provides detailed pinout and signal definitions for Memory Mode, I/O Mode and True IDE Mode CF Storage and CF+ Cards. Detailed functional and timing information is provided including the provision for reading 16-bit data on the low order 8 data bits (useful in 8-bit host systems) and the interpretation of status information returned by the CF Storage Card or CF+ Card.

2.4 Metaformat

This section describes the Card Information Structure (CIS), or Metaformat, on CompactFlash Storage Cards and CF+ Cards and how to interpret the Metaformat for the purpose of configuring and utilizing the card.

2.5 Software Interface

This section describes the software interface between the host and the CompactFlash Storage Card. This section does not apply to CF+ Cards.

2.6 CompactFlash Adapter

This section describes the passive Type II PCMCIA adapter that can be used with the Type I CompactFlash Storage Card or CF+ Card.

3 Card Physical

3.1 General Description

3.1.1 CompactFlash Storage Card

The CompactFlash Storage Card contains a single chip controller and flash memory module(s) in a matchbook-sized package with a 50-pin connector consisting of two rows of 25 female contacts each on 50 mil (1.27 mm) centers. The controller interfaces with a host system allowing data to be written to and read from the flash memory module(s).

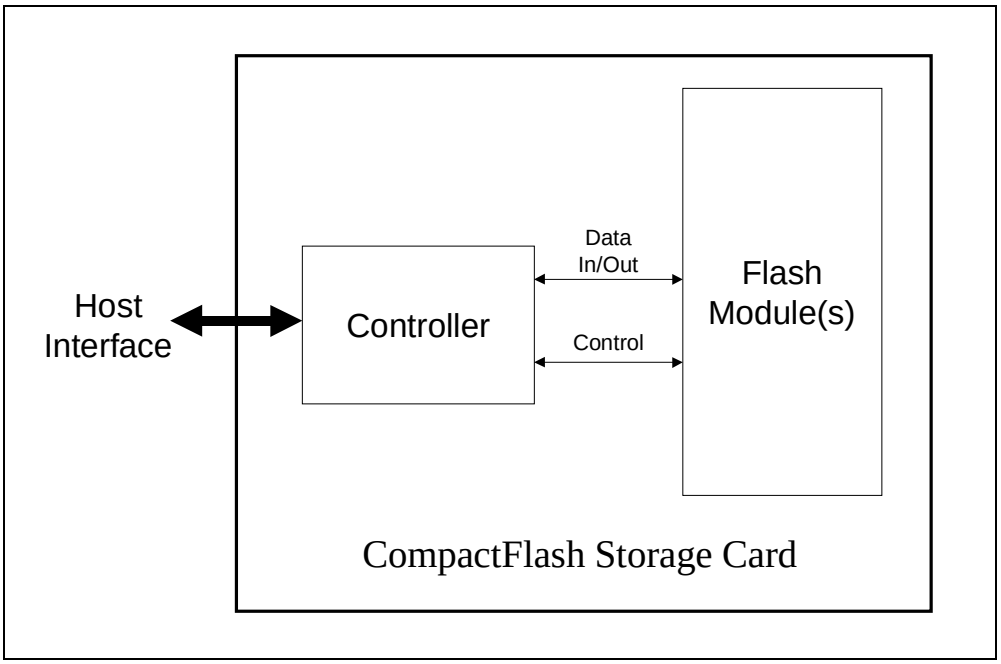


Figure 1: CompactFlash Storage Card Block Diagram

3.1.2 CF+ Card

The CF+ card contains functions other than ATA flash memory, such as I/O (serial port, modem, LAN, etc) or non-flash storage (hard disk drive). Physical specifications are identical to CompactFlash cards (either Type I or Type II).

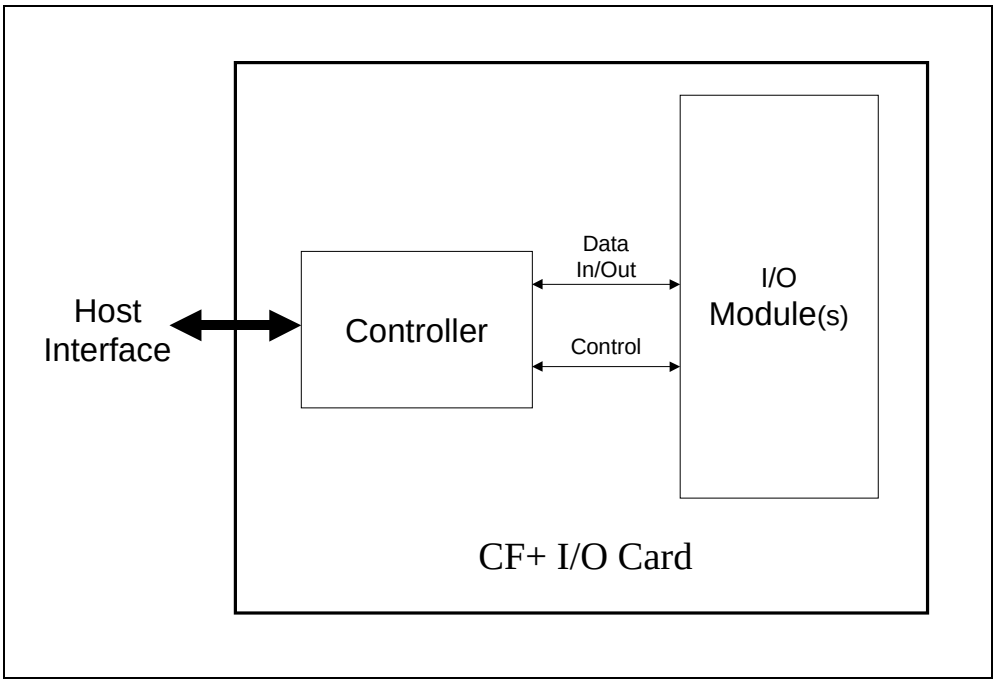


Figure 2: CF+ Card Block Diagram

3.2 CompactFlash Storage Card and CF+ Card Physical Specifications

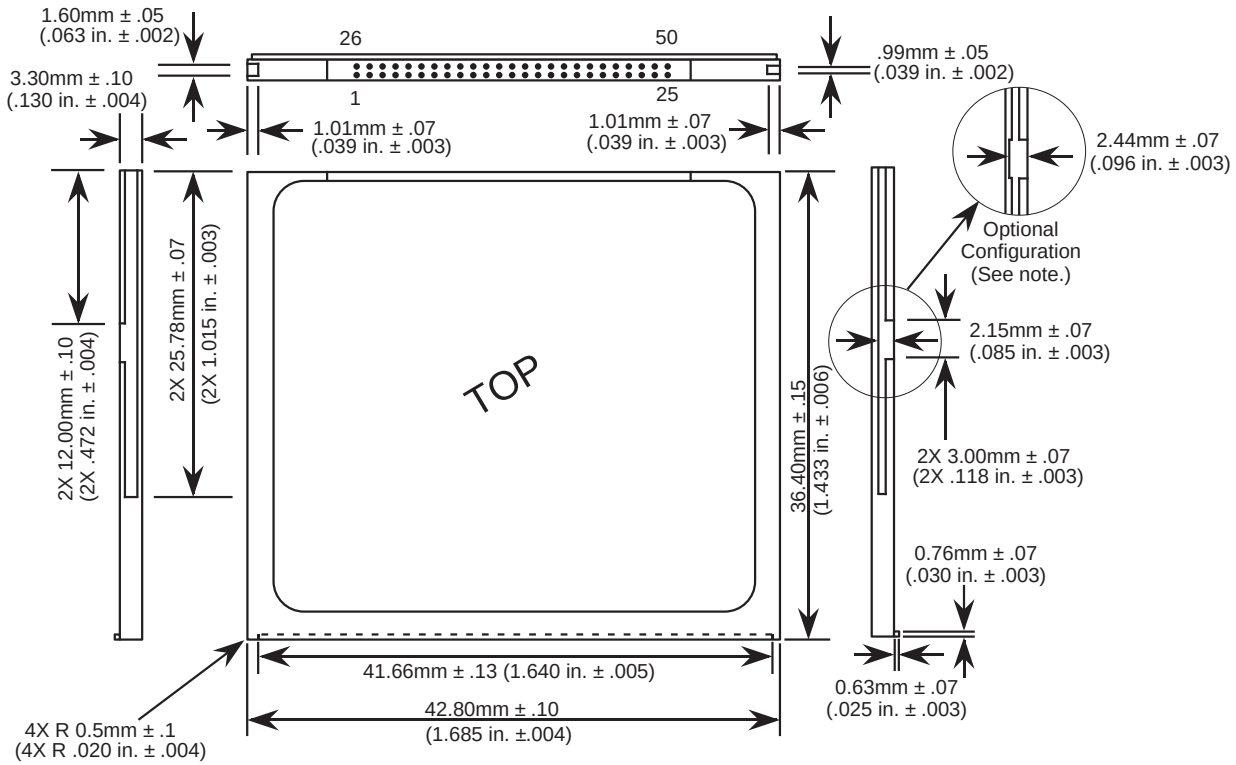
Refer to *Table 1*, *Table 2*, *Figure 3* and *Figure 4* for the CompactFlash Storage Card and the CF+ Card dimensions and physical specifications.

Table 1: Type I CompactFlash Storage Card and CF+ Card Physical Specifications

Length:	36.4 ± 0.15 mm (1.433 ±.006 in.)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in.)
Thickness Including Label Area:	3.3 mm ± 0.10 mm (.130 ± .004 in.)

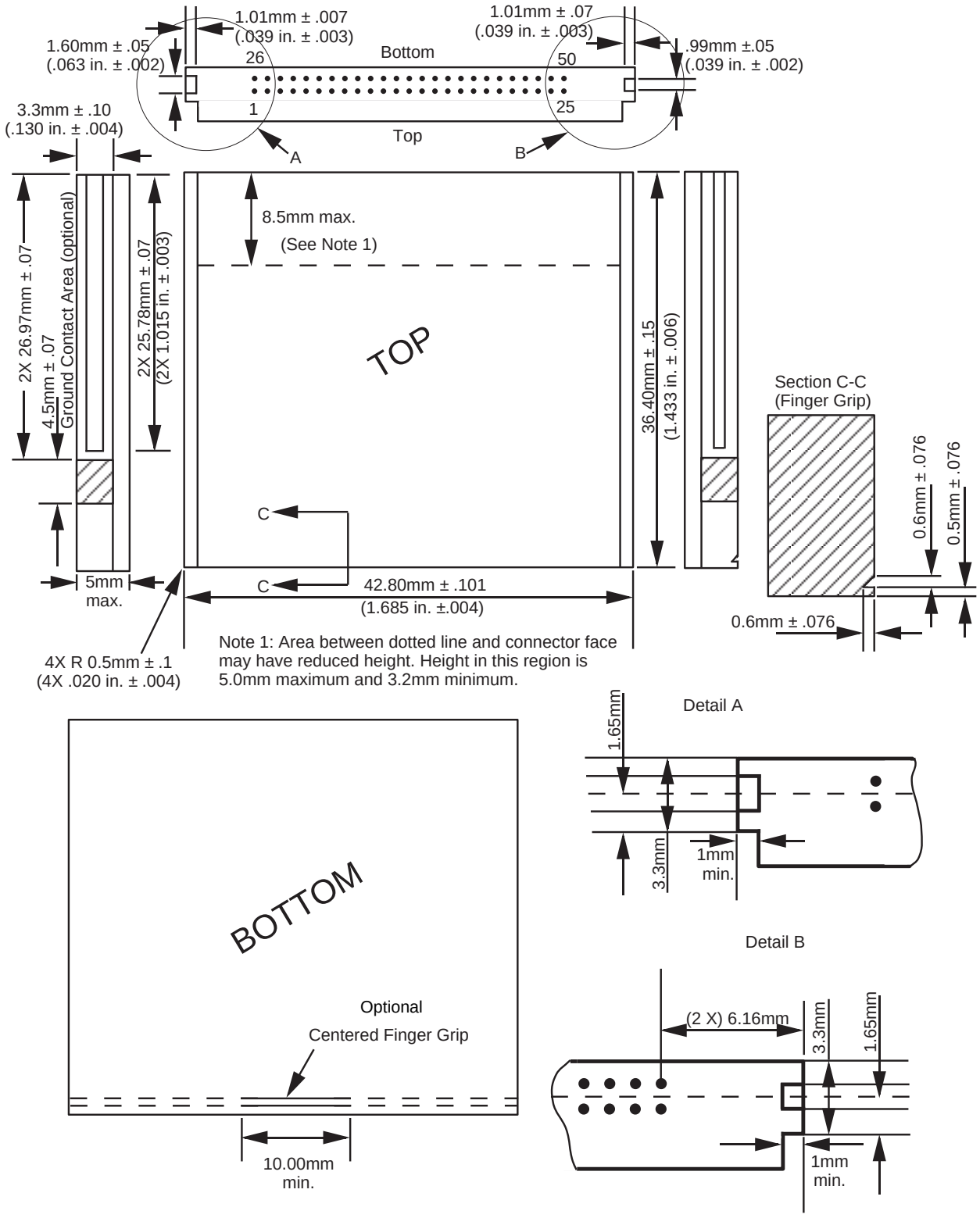
Table 2: Type II CompactFlash Storage Card and CF+ Card Physical Specifications

Length:	36.4 ± 0.15 mm (1.433 ±.006 in.)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in.)
Thickness Including Label Area:	5.0 mm maximum (.1968 in. maximum)



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

Figure 3: Type I CompactFlash Storage Card and CF+ Card Dimensions



Note: the recessed centered finger grip (Section C-C) is optional although it is recommended for CF+ Type II cards. Additionally, it is recommended that Type II host slots include an ejector mechanism.

Figure 4: Type II CompactFlash Storage Card and CF+ Card Dimensions

3.3 Connector Interface Specifications

The specified CF Card connector interface shall be a 50-position, 2-piece pin-and-socket. The socket contacts shall be within the CF Card connector. The outermost plating of the pin and socket contact areas shall be a noble metal that is compatible with gold, and shall meet the performance requirements specified in *Table 3: Connector Interface Requirement*.

Within this specification, the geometric plane established by the face of a fully engaged socket on its host connector is defined as "Datum A." To evaluate interchangeability among various connectors, dimensional layouts should be referenced from Datum A, i.e., the CF Card Socket face or the CF Card Slot Header floor.

Table 3: Connector Interface Requirement

Category	Item	Standard	Test Method
Physical	Housing Material	High Temperature Plastic	
	Housing Flammability Rating	UL 94V-0	Certification
Electrical Performance	Contact Resistance (w/ bulk)	40 milliohms maximum, initial 20 milliohms maximum change, throughout testing	EIA-364-23A
	Current Rating	0.5 Amperes per contact, without exceeding 30°C temperatire rise above ambient	IEC-512-PT3
	Insulation Resistance	1000 Megaohms minimum, initial 100 Megaohms minimum, after 1 minute @ 500 Vdc	EIA-364-21A
	Dielectric Withstanding Voltage	No shorting during 1 minute @ 500 Vac rms, with 1 mA maximum current leakage	EIA-364-20A
Mechnical Performance	Single Socket Holding Force	4.9 N minimum push out @ 25 mm/minute	EIA-364-29A
	Single Pin Holding Force	9.8 N minimum push out @ 25 mm/minute	EIA-364-29A
	Total Mating Force	28.8 N maximum at 25 mm/minute	EIA-364-13A
	Total Unmating Force	4.9 N minimum and 24.5 N maximum at 25 mm/minute	EIA-364-13A
	Durability	10,000 mating cycles, without exceeding low-level contact resistance	EIA-364-09B
Environmental Performance	Mechanical Shock	No discontinuities greater than 100 ns, Test Condition A	EIA-364-27A
	Vibration	No discontinuities greater than 100 ns, Test Condition III	EIA-364-28A
	Humidity	10 (24 hour) cycles with connector mated	EIA-364-31A
	Thermal Shock	-55°C to +85°C, 5 (1 hour) cycles	EIA-364-32B
	Mixed Flowing Gas	Environmental Class II for 96 hours with connector unmated	EIA-364-65

3.3.1 CF/CF+ Card Connector

The socket-connector shall be located in the CF/CF+ Card as shown in *Figure 3* and *Figure 4*. The CF/CF+ Card socket-connector interface layout shall match the host pin-connector layout as shown in *Figure 5*. The pin entry ports on the CF/CF+ Card socket-connector shall be configured as shown in *Figure 6*. The location of "first wipe on pin engagement" within the CF/CF+ Card socket-connector is shown in *Figure 7*.

The mechanical outlines for CF/CF+ Card Sockets are *Figure 8: Straddle Mount CF/CF+ Card Socket* and *Figure 9: Surface Mount CF/CF+ Card Socket*.

3.3.2 Host Connector

The host (CF/*CF+* Card slot) pin-connector shall be a 50-pin connector with opening, polarization, and pin location as shown in *Figure 10*. The pin size and shape shall be as shown in *Figure 11*. The type and length for each pin number is shown in *Figure 7*.

If the host is a Type II PCMCIA PC Card, the pin-connector must also conform to the physical specifications in Section 6.2 of the CompactFlash Adapter Specifications.

In all cases, the CF/*CF+* Card shall be guided by the host connector for a minimum of 6.5 mm before the socket connector fully seats on the host connector. To ensure alignment of the CF/*CF+* Card to the host connector, the CF/*CF+* Card shall be guided for a minimum distance of 19.0 mm before engagement.

The mechanical outlines for CF/*CF+* Card slot connectors are *Figure 12: Straddle Mount CF/CF+ Card Adapter Header* and *Figure 13: Surface Mount Right Angle CF/CF+ Type I Card Slot Header*. Recommended Pad or Hole PCB Patterns for various tail configurations and mounting methods are shown in *Figure 15* to *Figure 19*.

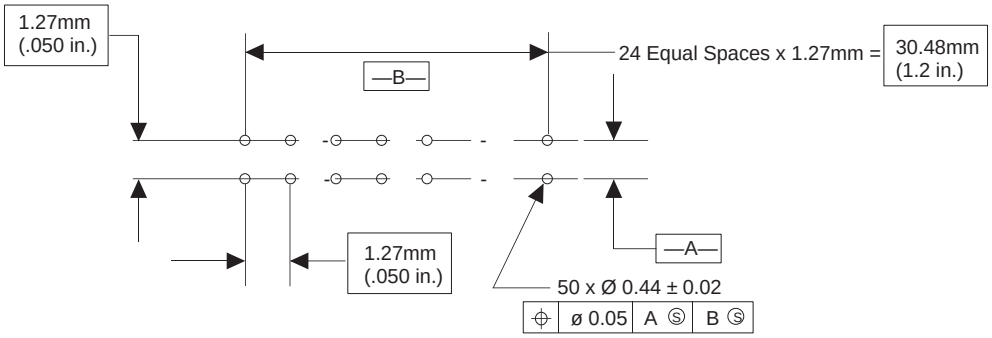


Figure 5: Position 2 Row Pin Pattern

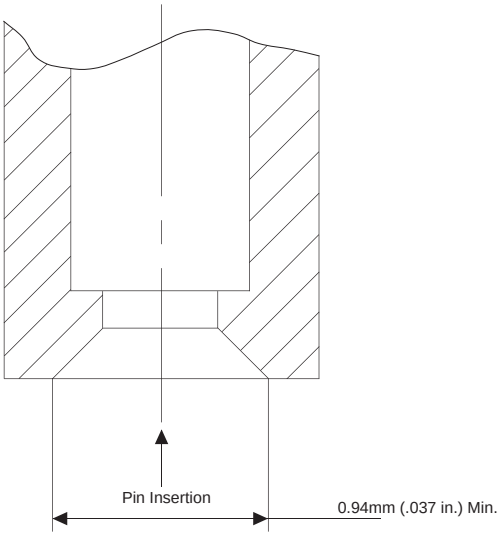
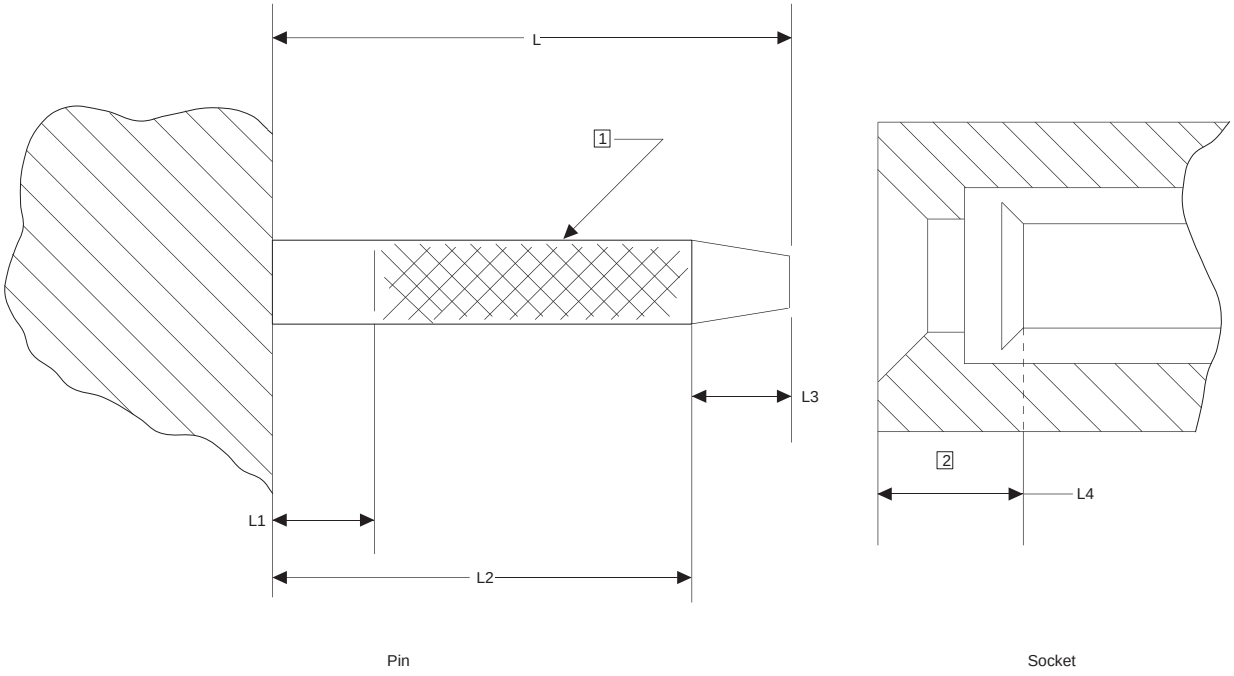


Figure 6: Socket Connector Entry

Description	Pin Number	L ± 0.10	L1 Max	L2 Ref	L3 ± 0.10	L4
Power	1, 13, 38 & 50	5.00 [.197]	0.50 [.020]	4.50 [.177]	0.50 [.020]	0.50 - 2.50 [.020 - .098]
General	All other pins	4.25 [.167]	0.50 [.020]	3.75 [.148]	0.50 [.020]	0.50 - 2.50 [.020 - .098]
Detect	25, 26	3.50 [.138]	0.50 [.020]	3.00 [.118]	0.50 [.020]	0.50 - 2.50 [.020 - .098]



Notes:
1 Pin/Socket contact area.
2 L4 is the point of first engagement for mating with the socket contacts/housing mounted within the card.

Figure 7: Pin and Socket Detail

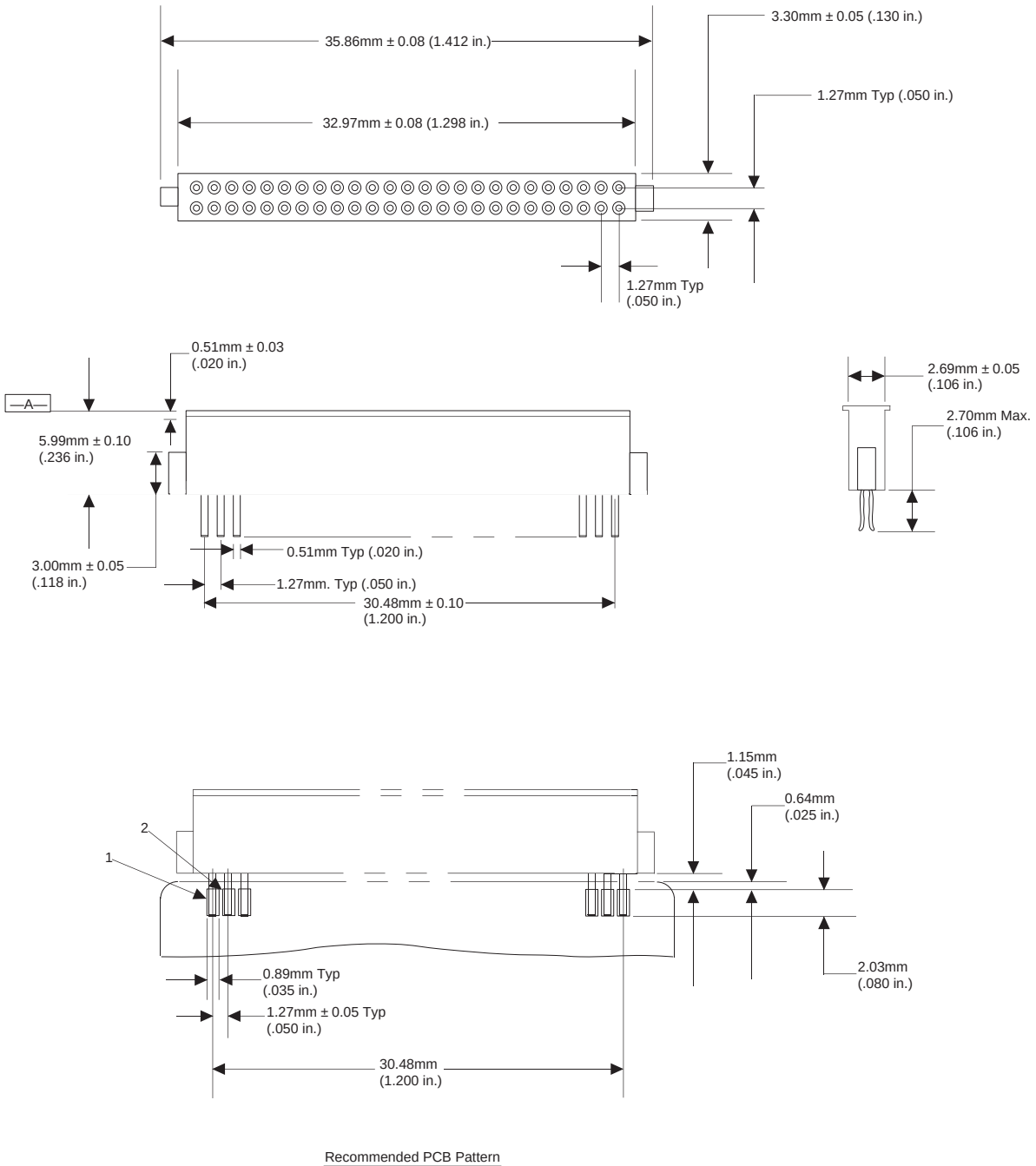


Figure 8: Straddle Mount CF/CF+ Card Socket

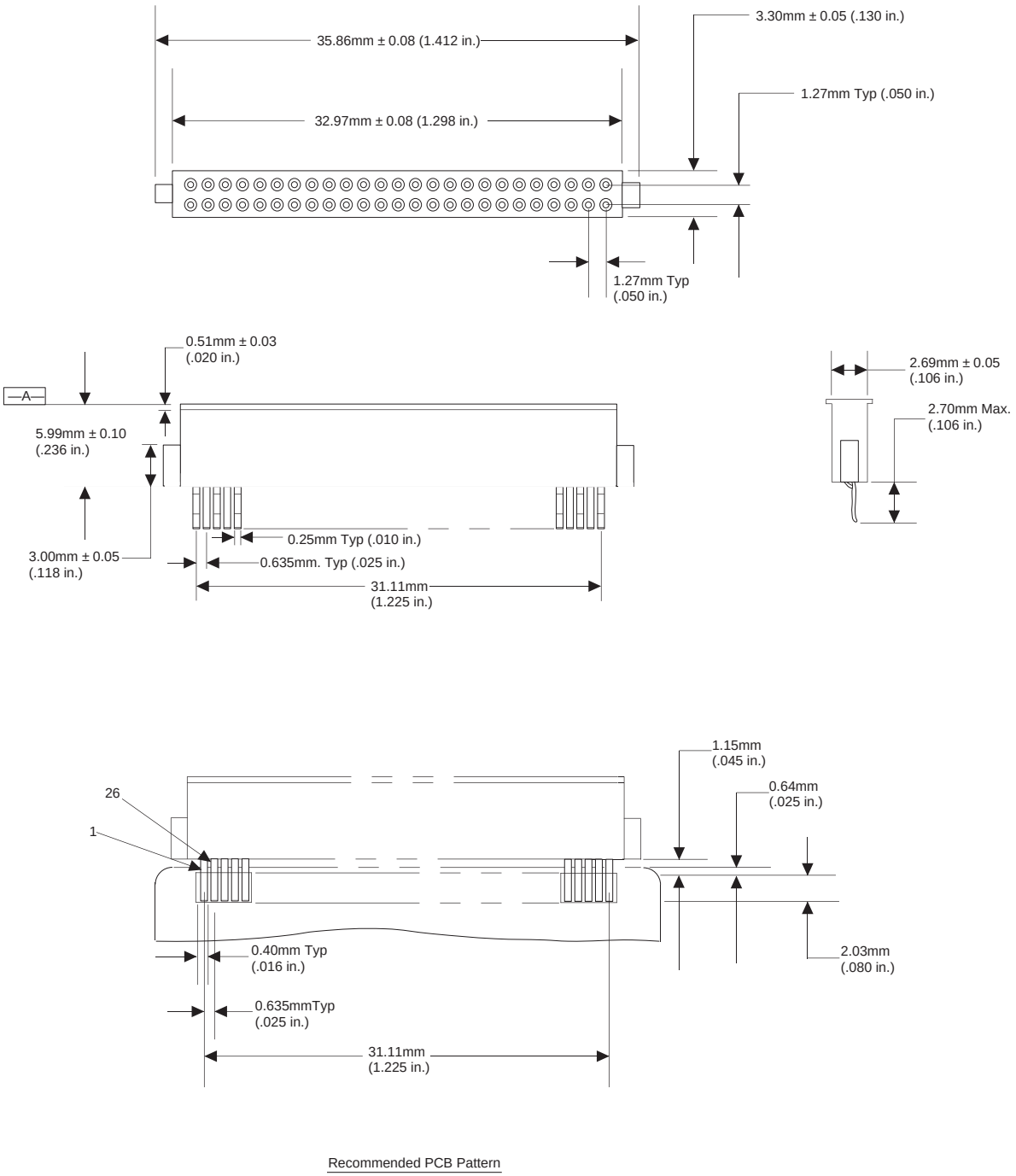


Figure 9: Surface Mount CF/CF+ Card Socket

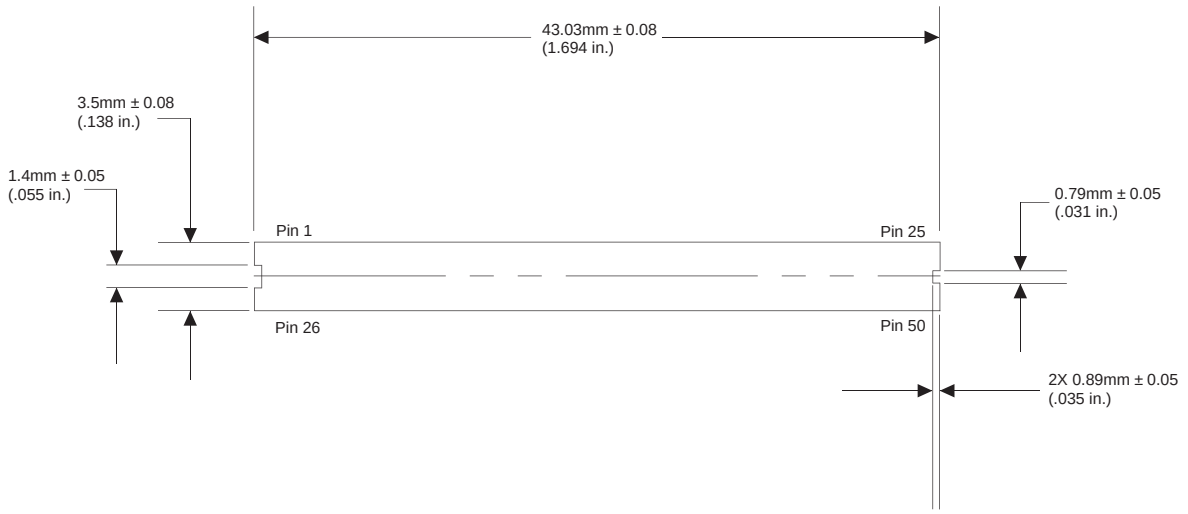


Figure 10: 50-Pin Connector Opening

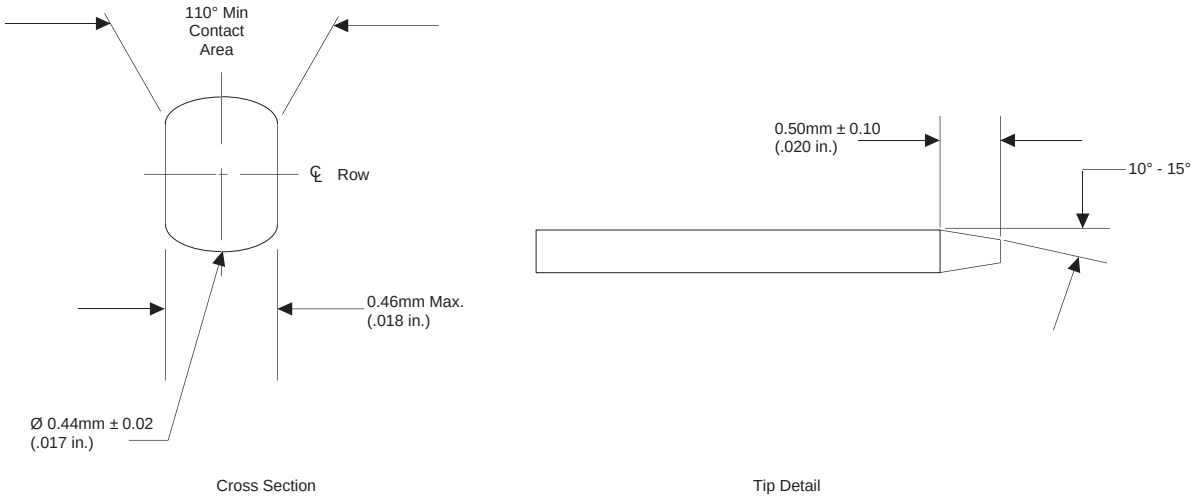


Figure 11: Header Pin Detail

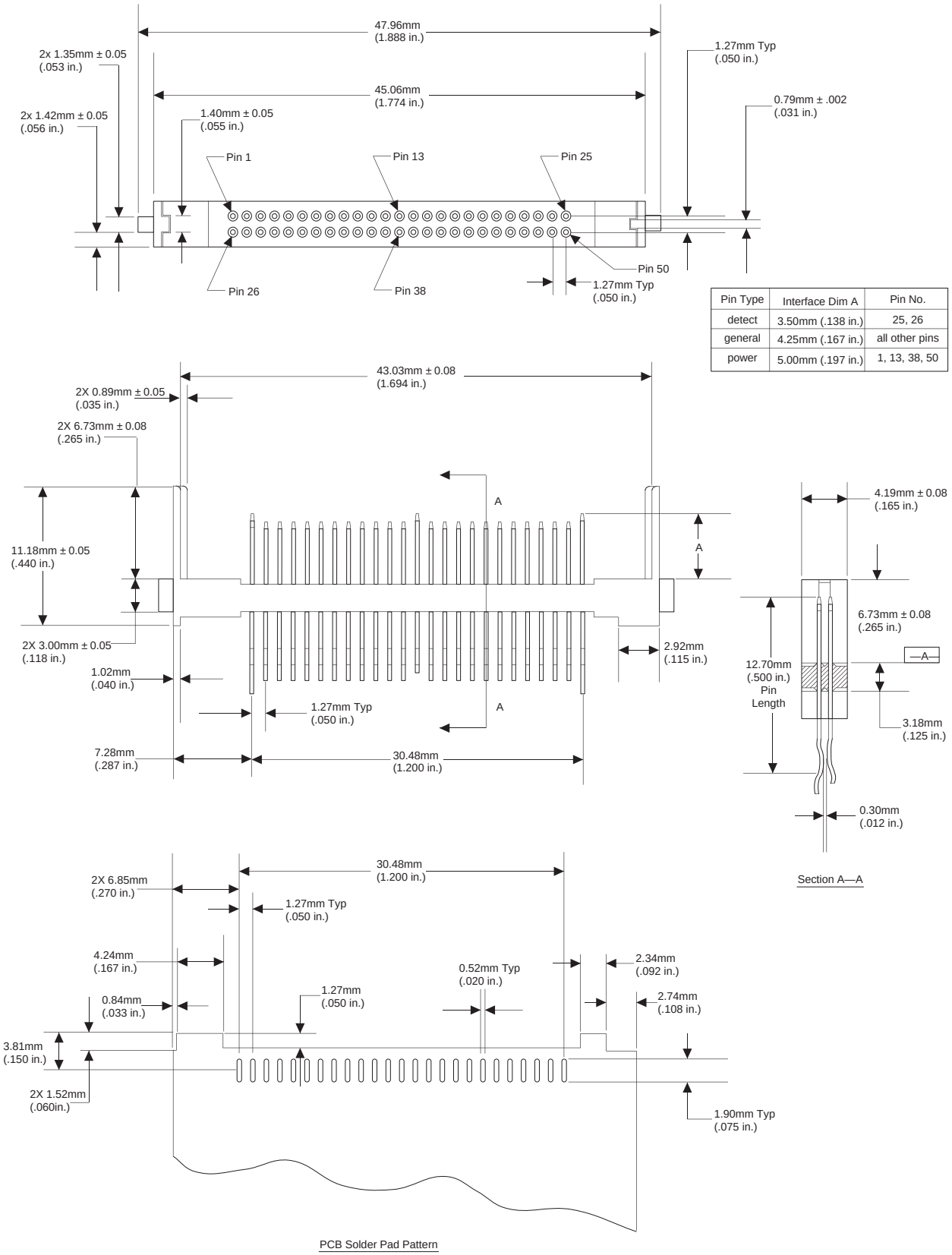


Figure 12: Straddle Mount CF/CF+ Card Adapter Header

Pin Type	Interface Dim A	Pin No.
detect	3.50mm (.138 in.)	25, 26
general	4.25mm (.167 in.)	all other pins
power	5.00mm (.197 in.)	1, 13, 38, 50

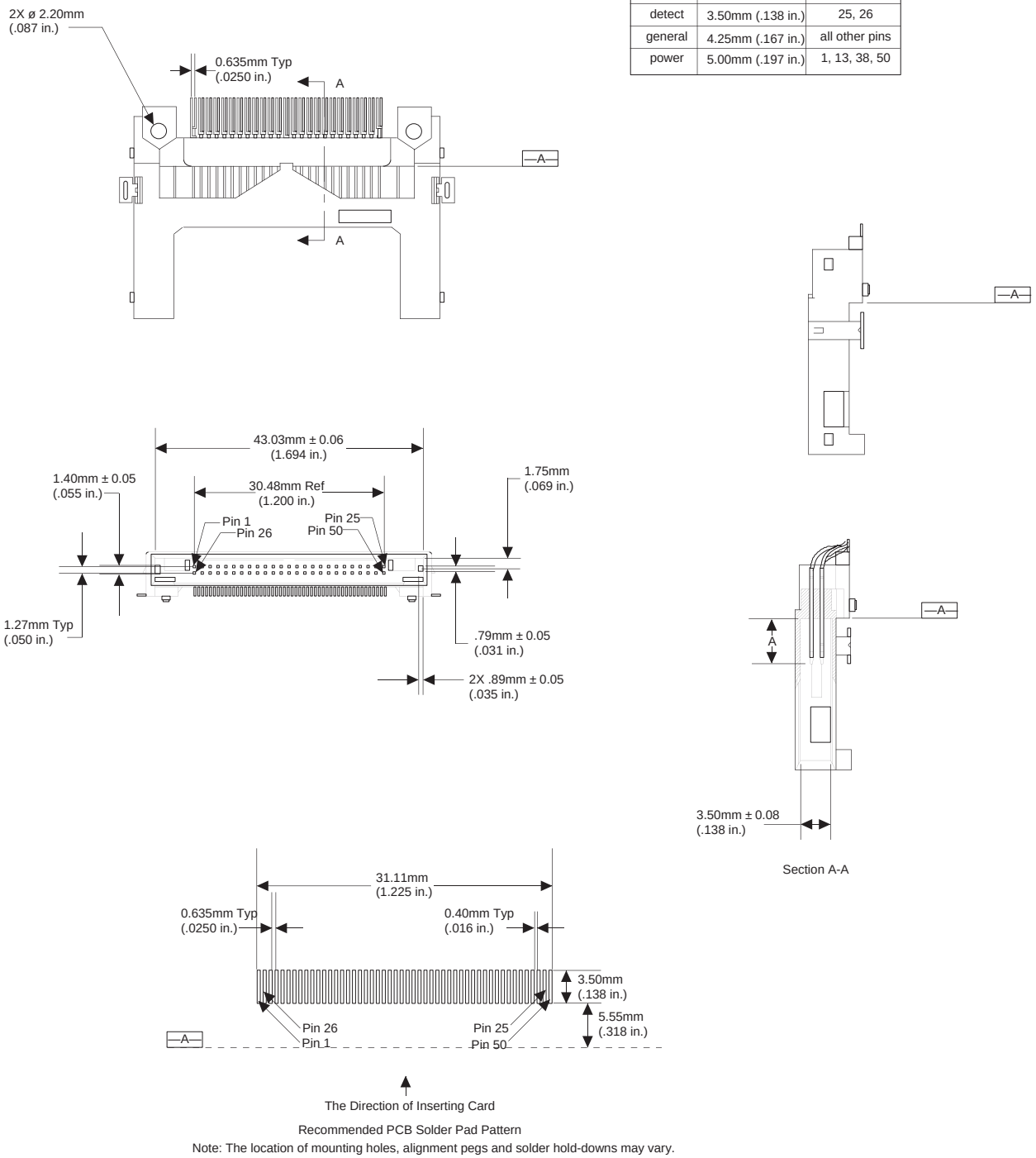


Figure 13: Surface Mount Right Angle CF/CF+ Type I Card Slot Header

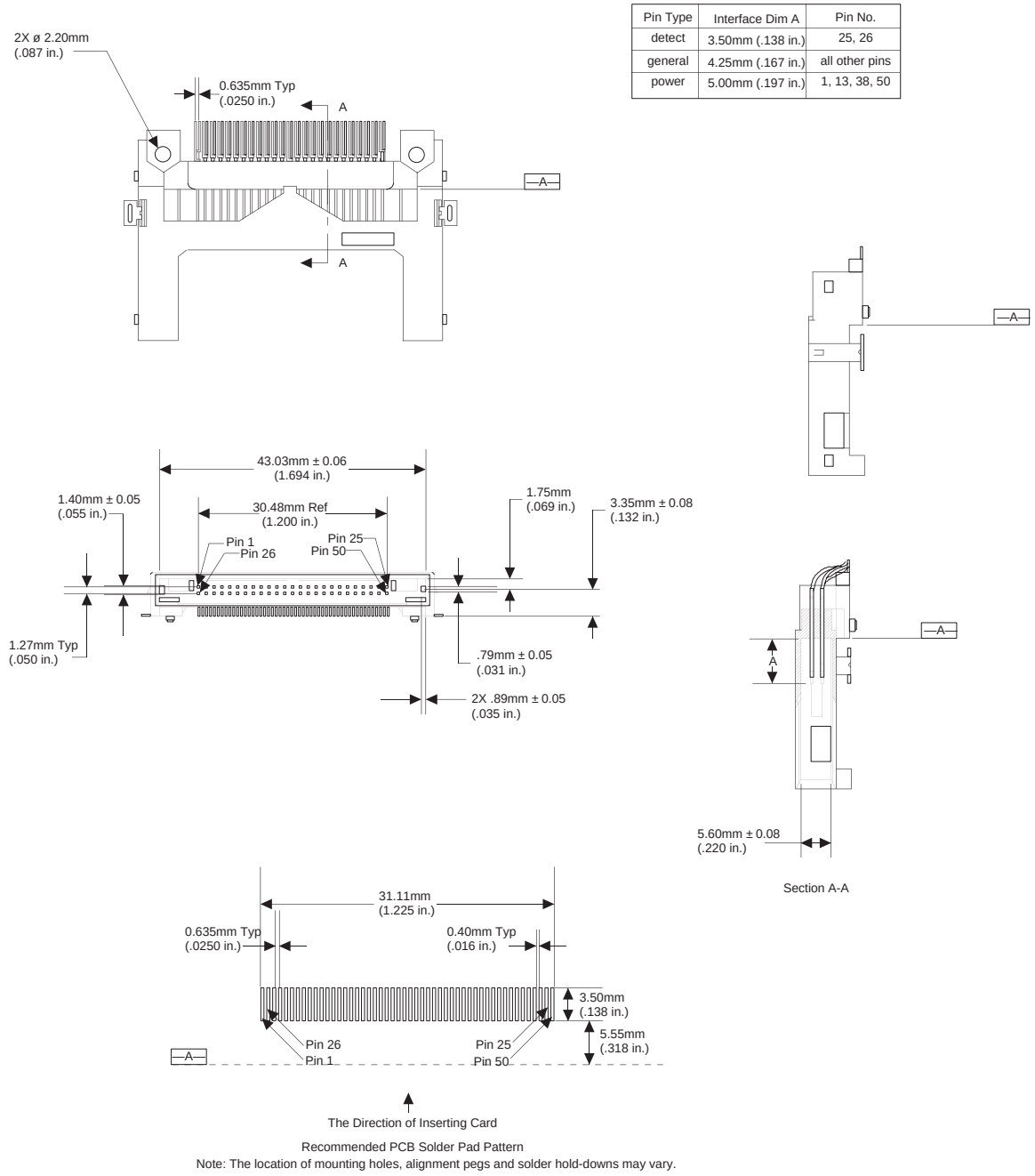


Figure 14: Surface Mount Right Angle CF/CF+ Type II Card Slot Header

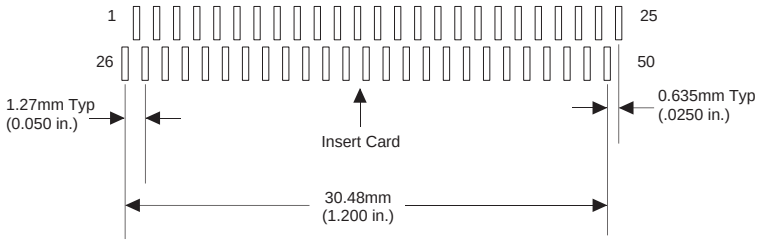


Figure 15: Two Row SMT Host PCB Pattern

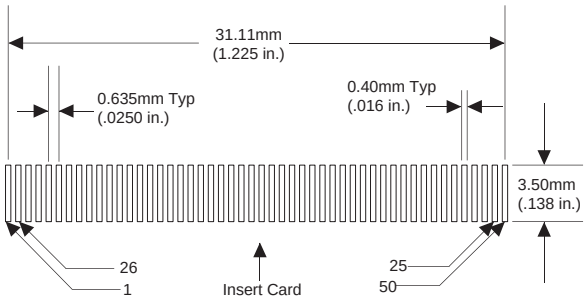


Figure 16: Single Row SMT Host PCB Pattern

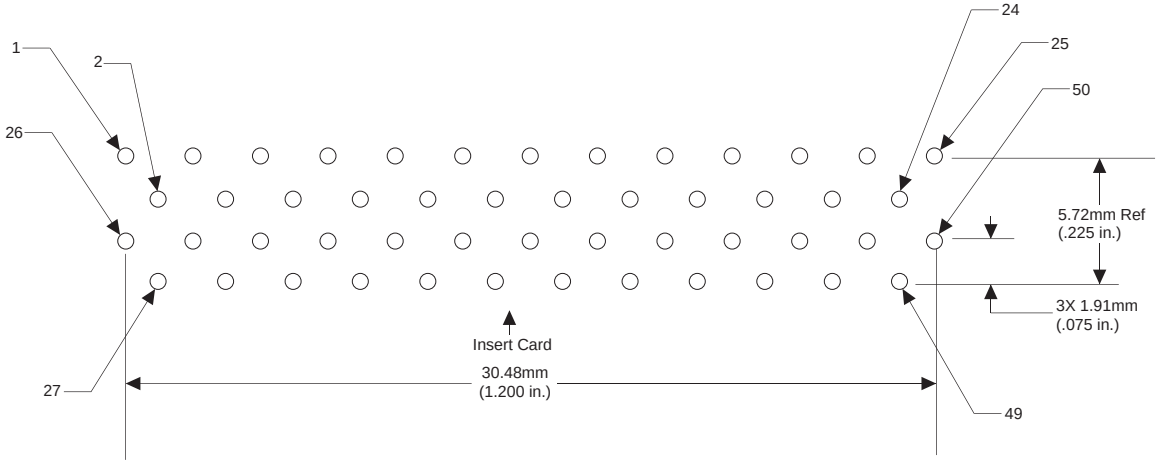


Figure 17: Right Angle Through Hole Host PCB Pattern

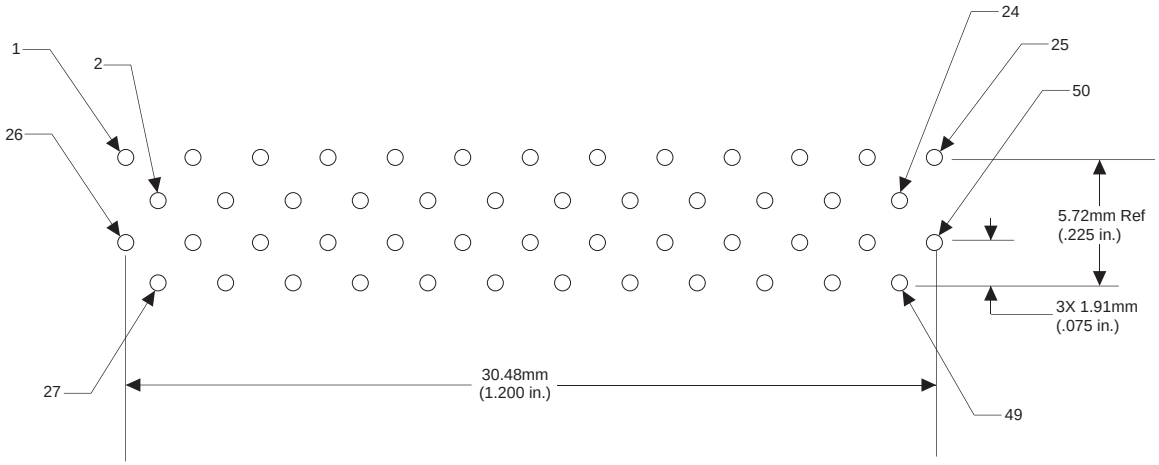


Figure 18: Vertical Through Hole Host PCB Pattern

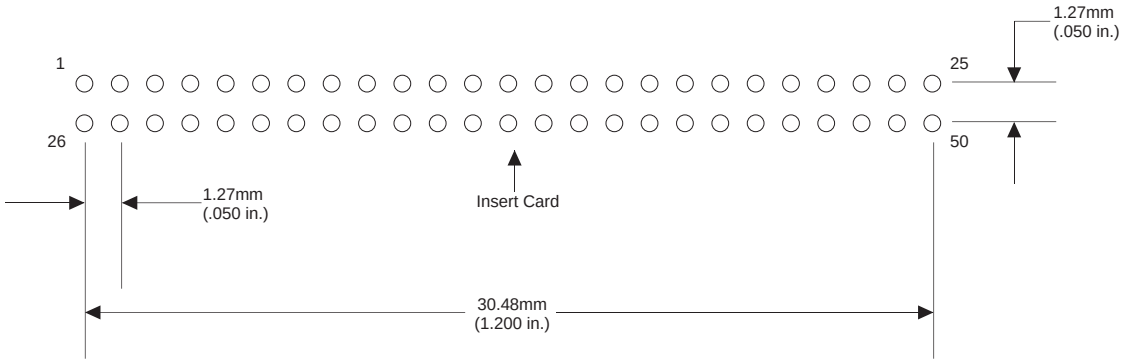


Figure 19: Alternate Right Angle Through Hole Host PCB Pattern

4 Electrical Interface

4.1 Physical Description

The host is connected to the CompactFlash Storage Card or CF+ Card using a standard 50-pin connector. The connector in the host consists of two rows of 25 male contacts each on 50 mil (1.27 mm) centers.

4.1.1 Pin Assignments and Pin Type

The signal/pin assignments are listed in *Table 4*. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. *Section 4.3* defines the DC characteristics for all input and output type structures.

4.2 Electrical Description

The CompactFlash Storage Card functions in three basic modes: 1) PC Card ATA using I/O Mode, 2) PC Card ATA using Memory Mode and 3) True IDE Mode, which is compatible with most disk drives. CompactFlash Storage Cards are required to support all three modes. The CF+ Cards normally function in the first and second modes, however they can optionally function in True IDE mode. The configuration of the CompactFlash Card will be controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the storage card or for True IDE Mode, pin 9 being grounded. The configuration of the CF+ Card will be controlled using configuration registers starting at the address defined in the Configuration Tuple (CISTPL_CONFIG) in the Attribute Memory space of the CF+ Card.

Table 5 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the CompactFlash Storage Card or CF+ Card sources are outputs. The CompactFlash Storage Card and CF+ Card logic levels conform to those specified in the PCMCIA Release 2.1 specification. In *Table 5*, each signal has three possible operating modes: 1) PC Card Memory, 2) PC Card I/O and 3) True IDE. True IDE mode is required for CompactFlash Storage cards, and optional for CF+ Cards. All outputs from the card are totempole except the data bus signals that are bi-directional tri-state. Refer to *Section 4.3* for definitions of Input and Output type.

Table 4: Pin Assignments and Pin Type

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10[2]	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09[2]	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08[2]	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07[2]	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06[2]	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05[2]	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04[2]	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03[2]	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3
23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3	27	D11[1]	I/O	I1Z,OZ3
28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3	28	D12[1]	I/O	I1Z,OZ3
29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3	29	D13[1]	I/O	I1Z,OZ3
30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3	30	D14[1]	I/O	I1Z,OZ3
31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3	31	D15[1]	I/O	I1Z,OZ3
32	-CE2[1]	I	I3U	32	-CE2[1]	I	I3U	32	-CS1[1]	I	I1Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD	I	I3U	34	-IORD	I	I3U	34	-IORD	I	I3Z
35	-IOWR	I	I3U	35	-IOWR	I	I3U	35	-IOWR	I	I3Z
36	-WE	I	I3U	36	-WE	I	I3U	36	-WE[3]	I	I3U

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode[4]			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
37	RDY/BSY	O	OT1	37	IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	-CSEL	I	I2Z	39	-CSEL	I	I2Z	39	-CSEL	I	I2U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	-RESET	I	I2Z
42	-WAIT	O	OT1	42	-WAIT	O	OT1	42	IORDY	O	ON1
43	-INPACK	O	OT1	43	-INPACK	O	OT1	43	-INPACK	O	OZ1
44	-REG	I	I3U	44	-REG	I	I3U	44	-REG[3]	I	I3U
45	BVD2	I/O	I1U,OT1	45	-SPKR	I/O	I1U,OT1	45	-DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U,OT1	46	-STSCHG	I/O	I1U,OT1	46	-PDIAG	I/O	I1U,ON1
47	D08[1]	I/O	I1Z,OZ3	47	D08[1]	I/O	I1Z,OZ3	47	D08[1]	I/O	I1Z,OZ3
48	D09[1]	I/O	I1Z,OZ3	48	D09[1]	I/O	I1Z,OZ3	48	D09[1]	I/O	I1Z,OZ3
49	D10[1]	I/O	I1Z,OZ3	49	D10[1]	I/O	I1Z,OZ3	49	D10[1]	I/O	I1Z,OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

Note: 1. These signals are required only for 16 bit access and not required when installed in 8-bit systems. Devices should allow for 3-state signals not to consume current.

2. Should be grounded by the host.

3. Should be tied to VCC by the host.

4. Optional for CF+ Cards, required for CompactFlash Storage Cards.

Table 5: Signal Description

Signal Name	Dir.	Pin	Description
A10 - A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
A10 - A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode)	I	18,19,20	In True IDE Mode only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. –CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Tables 4-11, 4-12, 4-15, 4-16 and 4-17.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.

Signal Name	Dir.	Pin	Description
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This signal is not used for this mode.
-CSEL (True IDE Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15 - D00 (PC Card Memory Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15 - D00 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
D15 - D00 (True IDE Mode)			In True IDE Mode, all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.
GND (PC Card Memory Mode)	--	1,50	Ground.
GND (PC Card I/O Mode)			This signal is the same for all modes.
GND (True IDE Mode)			This signal is the same for all modes.
-INPACK (PC Card Memory Mode)	O	43	This signal is not used in this mode.
-INPACK (PC Card I/O Mode) Input Acknowledge			The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU.
-INPACK (True IDE Mode)			In True IDE Mode this output signal is not used and should not be connected at the host.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Signal Name	Dir.	Pin	Description
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
RDY/-BSY (PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor.
			At power up and at Reset, the RDY/-BSY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash Storage Card or CF+ Card has been powered up with +RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)			I/O Operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
RESET (PC Card Memory Mode)	I	41	When the pin is high, this signal Resets the CompactFlash Storage Card or CF+ Card. The CompactFlash Storage Card or CF+ Card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
-RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	--	13,38	+5 V, +3.3 V power.
VCC (PC Card I/O Mode)			This signal is the same for all modes.
VCC (True IDE Mode)			This signal is the same for all modes.

Signal Name	Dir.	Pin	Description
-VS1 -VS2 (PC Card Memory Mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded so that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage.
-VS1 -VS2 (PC Card I/O Mode)			This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)			This signal is the same for all modes.
-WAIT (PC Card Memory Mode)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
-WAIT (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
IORDY (True IDE Mode)			In True IDE Mode this output signal may be used as IORDY.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect	O	24	Memory Mode – The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation – When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

4.3 Electrical Specification

Table 6 defines all D.C. Characteristics for the CompactFlash Storage Card and CF+ Card Series. Unless otherwise stated, conditions are:

Vcc = 5V ±10%

Vcc = 3.3V ± 5%

Ta = 0°C to 60°C

Table 6: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	Vcc	-0.3V min. to 6.5V max.
Voltage on any pin except Vcc with respect to GND.	V	-0.5V min. to Vcc + 0.5V max.

Table 7: Input Power

Voltage	Maximum Average RMS Current	Measurement Method
3.3V ± 5%	75 mA (500mA in Power Level 1)	3.3V at 25°C
5.0V ± 10%	100 mA (500mA in Power Level 1)	5.0V at 25°C

CompactFlash and CF+ products shall operate correctly in both voltage ranges as shown in the table above. To comply with this specification, current requirements must not exceed the maximum limit.

The maximum average RMS current for CompactFlash cards is 75 mA at 3.3V and 100 mA at 5V. For CF+ cards, two power levels are defined. Power Level 0 has the same current specifications as CompactFlash cards, while Power Level 1 has an increased maximum current of 500 mA for both 3.3V and 5V.

CF+ cards must operate within the specifications for Power Level 0 at power on and after reset. CF+ cards must also support CIS reads and (for ATA CF+ cards only) ATA Identify Device commands in Power Level 0. This requirement allows the host device to determine whether the CF+ card has commands which require Power Level 1 (see *Sections 5.2* and *6.2.1.5.25*). If the host cannot support Power Level 1, the host can either disable Power Level 1 commands in the CF+ card (see *Sections 4.4.5* and *6.2.1.23*) or reject the CF+ card.

An example of a CF+ card using both Power Level 0 and Power Level 1 is a disk drive. Typically, commands which require the spindle to rotate (e.g., read/write commands) will be Power Level 1 commands. CF+ disk drives must make provisions to accommodate the execution of CIS reads and ATA Identify Device commands in Power Level 0; that is, without rotating the spindle.

4.3.1 Current Measurement

For Compact Flash Storage Cards, current measurement is accomplished by connecting an amp meter (set to the 2 amp scale range) with a fast current probe with an RC filter with a time constant of 0.1 msec, in series with the Vcc supply to the CompactFlash Storage Card. Current measurements are to be taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in the above *Table 6*.

For CF+ cards, a fast (>1 MHz) current probe monitors current on the Vcc supply to the CF+ card. The output of the current probe is filtered by an RC filter with a time constant of 0.1 msec. The output of the filter is monitored with a fast (>1 MHz) scope or other monitor. The filtered output measured in this way shall not exceed the specifications shown for Power Level 0 (for all CF+ cards) and for Power Level 1 (for CF+ cards supporting Power Level 1).

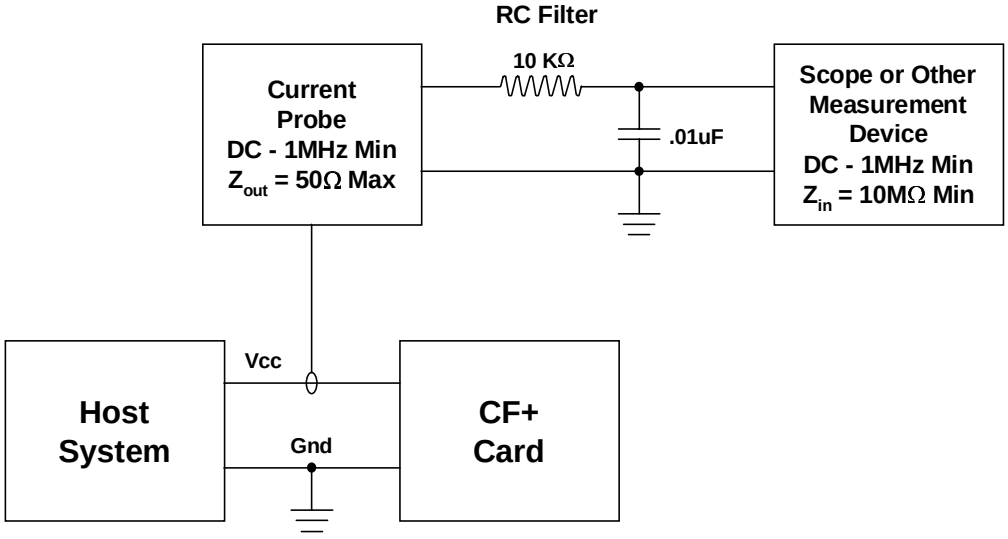


Figure 20: CF+ Power Supply Current Measurement Method

4.3.2 Input Leakage Current

Note: In *Table 8* below, x refers to the characteristics described in *Section 4.3.3*. For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Table 8: Input Leakage Current

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
IxZ	Input Leakage Current	IL	Vih = Vcc / Vil = Gnd	-1		1	µA
IxU	Pull Up Resistor	RPU1	Vcc = 5.0V	50k		500k	Ohm
IxD	Pull Down Resistor	RPD1	Vcc = 5.0V	50k		500k	Ohm

Note: The minimum pull up resistor leakage current meets the PCMCIA specification of 10k ohms but is intentionally higher in the CompactFlash Specification to reduce power use.

4.3.3 Input Characteristics

Table 9: Input Characteristics

Type	Parameter	Symbol	MIN	TYP	MAX	MIN	TYP	MAX	Units
			VCC = 3.3 V			VCC = 5.0 V			
1	Input Voltage CMOS	Vih Vil	2.4		0.6	4.0 [2]		0.8	Volts
2	Input Voltage CMOS	Vih Vil	1.5		0.6	2.0		0.8	Volts
3	Input Voltage CMOS Schmitt Trigger	Vth Vtl		1.8 1.0			2.8 2.0		Volts

4.3.4 Output Drive Type

Note: In *Table 10* below, x refers to the characteristics described in *Section 4.3.5*. For example, OT3 refers to Totempole output with a type 3 output drive characteristic.

Table 10: Output Drive Type

Type	Output Type	Valid Conditions
OTx	Totempole	Ioh & Iol
OZx	Tri-State N-P Channel	Ioh & Iol
OPx	P-Channel Only	Ioh Only
ONx	N-Channel Only	Iol Only

[2] Per PCMCIA Electrical Specification Signal Interface Table 4-18 note 1, the host must provide a logic output high voltage for a CMOS load of .9 x VCC. For a 5 volt product, this translates to .9 x 4.5 = 4.05 volts minimum Voh.

4.3.5 Output Drive Characteristics

Table 11: Output Drive Characteristics

Type	Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
1	Output Voltage	Voh Vol	Ioh = -4 mA Iol = 4 mA	Vcc -0.8V		 Gnd +0.4V	Volts
2	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 Gnd +0.4V	Volts
3	Output Voltage	Voh Vol	Ioh = -8 mA Iol = 8 mA	Vcc -0.8V		 Gnd +0.4V	Volts
X	Tri-State Leakage Current	Ioz	Vol = Gnd Voh = Vcc	-10		10	µA

4.3.6 Signal Interface

Electrical specifications must be maintained to ensure data reliability.

Table 12: Electrical Interface

Item	Signal	Card	Host
Control Signal	CE1# CE2# REG# IORD# IOWR#	Pull-up to Vcc R ≥ 10 KΩ and must be sufficient to keep inputs inactive when the pins are not connected at the host.[3]	
	OE# WE#	Pull-up to Vcc R ≥ 10 KΩ.[3,4]	
	RESET	Pull-up to Vcc R ≥ 10 KΩ.[3,4]	
Status Signal	READY INPACK# WAIT# WP#		Pull-up to Vcc R ≥ 10 KΩ.[5]
Address	A[11::0]	Pull-down R ≥ 100 KΩ.[4,6]	
Data Bus	D[15::0]	Pull-down R ≥ 100 KΩ.[4,7]	
Card Detect	CD[2::1]#	Connected to GND in the card	
Voltage Sense	VS1# VS2#		Pull-up to Vcc 10 KΩ ≤ R 100KΩ.
Battery/Detect	BVD[2::1]		Pull-up[8]

[3] Control Signals: each card shall present a load to the socket no larger than 50pF at a DC current of 700μA low state and 150μA high state, including pull-resistor. The socket shall be able to drive at least the following load while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (50pF with DC current 700μA low state and 150μA high state per socket).

[4] Resistor is optional.

[5] Status Signals: the socket shall present a load to the card no larger than 50pF at a DC current of 400μA low state and 100μA high state, including pull-up resistor. The card shall be able to drive at least the following load while meeting all AC timing requirements: 50pF at a DC current of 400μA low state and 100μA high state.

[6] Address Signals: each card shall present a load of no more than 100pF at a DC current of 450μA low state and 150μA high state. The host shall be able to drive at least the following load while meeting all AC timing requirements: (the number of sockets wired in parallel) multiplied by (100pF with DC current 450μA low state and 150μA high state per socket).

[7] Data Signals: the host and each card shall present a load no larger than 50pF at a DC current of 450μA and 150μA high state. The host and each card shall be able to drive at least the following load while meeting all AC timing requirements: 100pF with DC current 1.6mA low state and 300μA high state. This permits the host to wire two sockets in parallel without derating the card access speeds.

[8] **BVD2** was not defined in the JEIDA 3.0 release. Systems fully supporting JEIDA release 3 STAM cards must pull-up pin 45 (**BVD2**) to avoid sensing their batteries as "Low."

4.3.7 Interface/Bus Timing

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, direct mapped I/O transfer and memory access. The two timing sequences are detailed in the PCMCIA PC Card Standard. The CompactFlash Storage Card and CF+ Card conform to the timing in that reference document.

4.3.8 Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300ns. Detailed timing specs are shown in *Table 13*.

Table 13: Attribute Memory Read Timing

Speed Version			300 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns.**	**Max ns.**
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

Note: All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

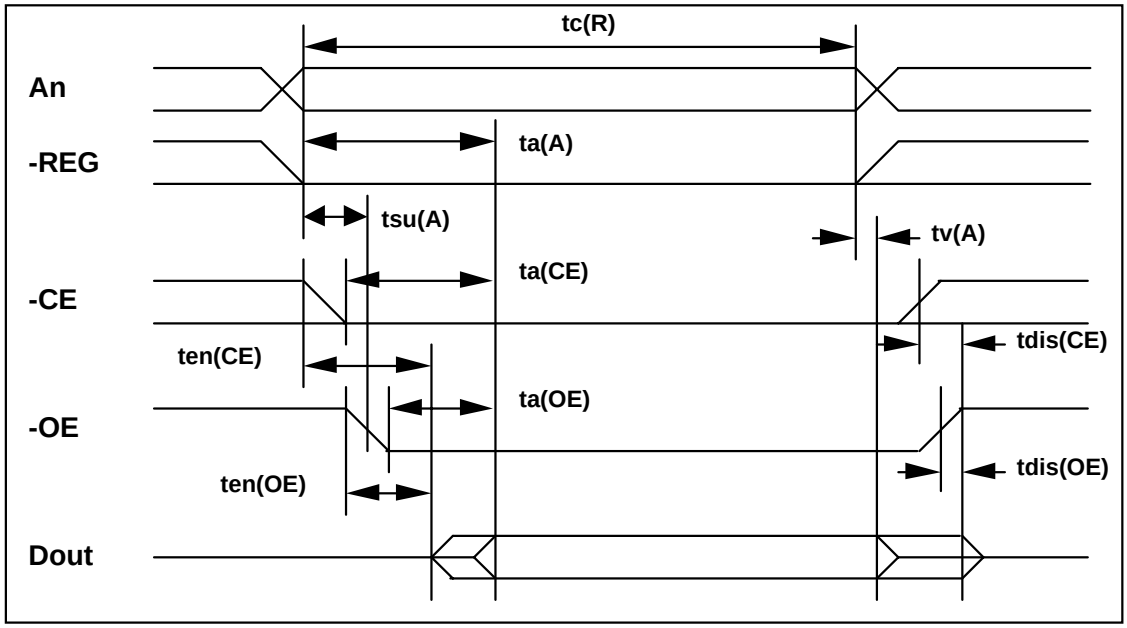


Figure 21: Attribute Memory Read Timing Diagram

4.3.9 Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250ns. Detailed timing specifications are shown in *Table 14*.

Table 14: Configuration Register (Attribute Memory) Write Timing

Speed Version			250 ns	
Item	**Symbol**	**IEEE Symbol**	**Min ns**	**Max ns**
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

Note: All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card.

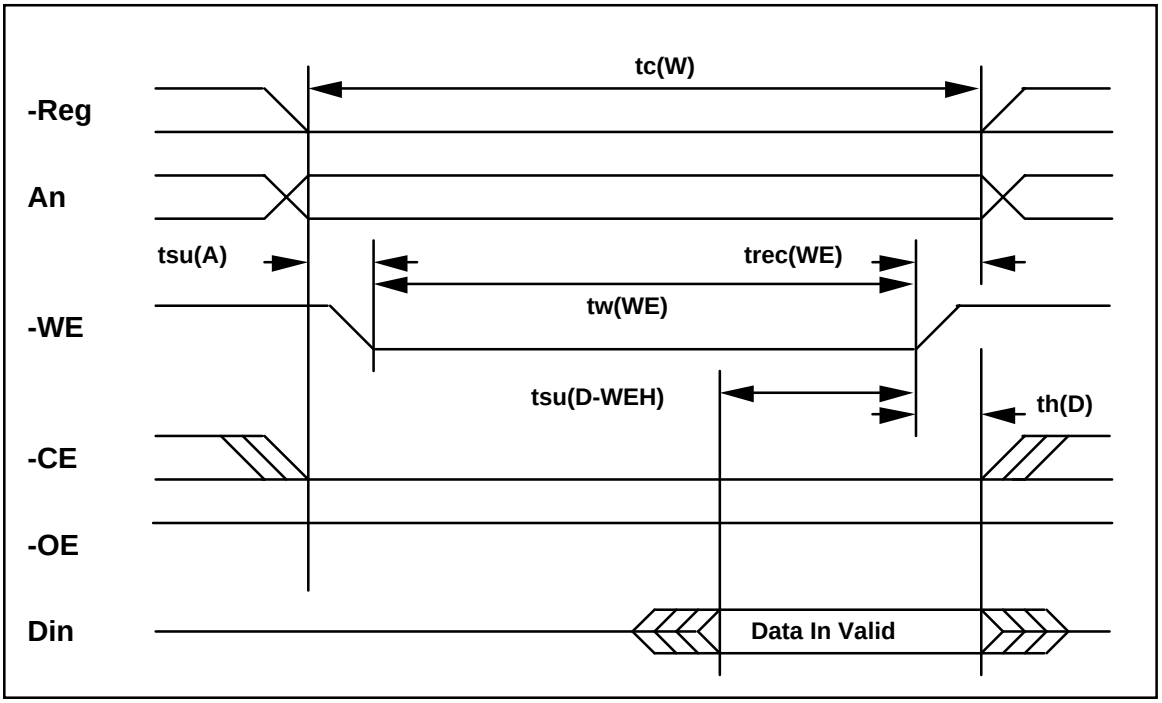


Figure 22: Configuration Register (Attribute Memory) Write Timing Diagram

4.3.10 Common Memory Read Timing Specification

Table 15: Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Address Hold Time	th(A)	tGHAX	20	
CE Setup before OE	tsu(CE)	tELGL	0	
CE Hold following OE	th(CE)	tGHEH	20	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35
Data Setup for Wait Release	tv(WT)	tQVWTH		0
Wait Width Time	tw(WT)	tWTLWTH		350 (3000 for *CF+*)

Note: The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

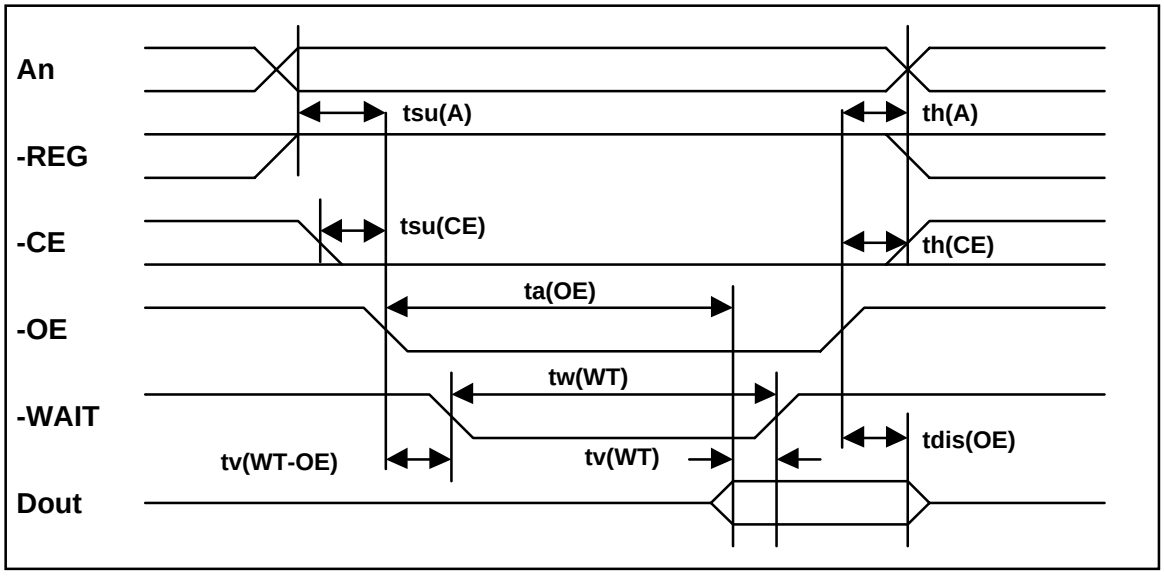


Figure 23: Common Memory Read Timing Diagram

4.3.11 Common Memory Write Timing Specification

Table 16: Common Memory Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before WE	tsu(D-WEH)	tDVWH	80	
Data Hold following WE	th(D)	tWMDX	30	
WE Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
CE Setup before WE	tsu(CE)	tELWL	0	
Write Recovery Time	trec(WE)	tWMAX	30	
Address Hold Time	th(A)	tGHAX	20	
CE Hold following WE	th(CE)	tGHEH	20	
Wait Delay Falling from WE	tv(WT-WE)	tWLWTV		35
WE High from Wait Release	tv(WT)	tWTHWH	0	
Wait Width Time	tw (WT)	tWTLWTH		350 (3000 for *CF+*)

Note: The maximum load on -WAIT is 1 LSTTL with 50pF total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

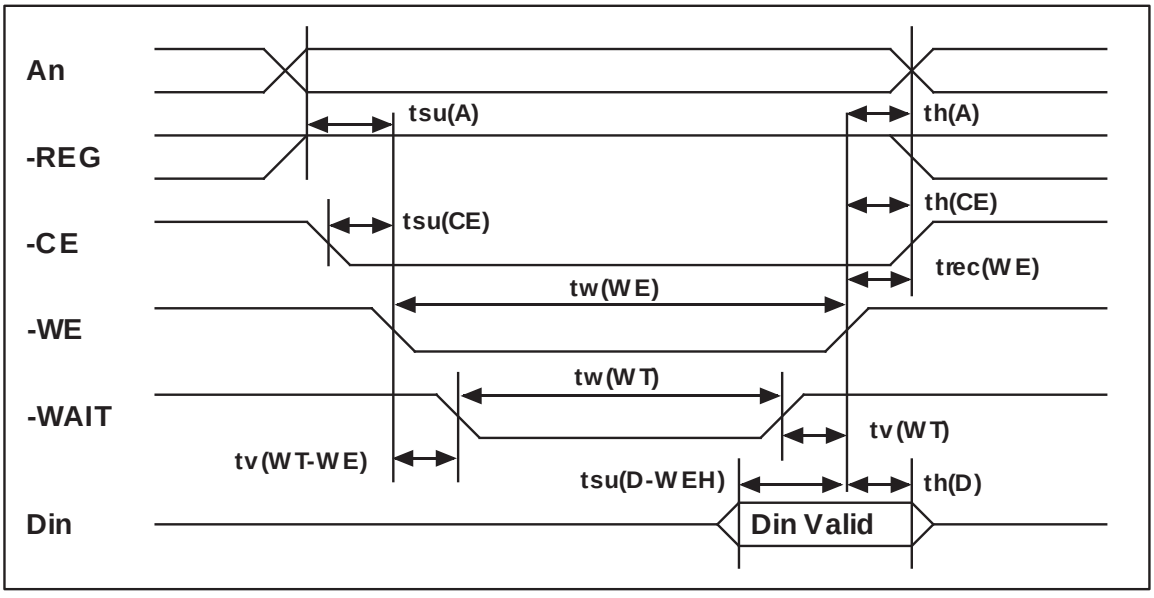


Figure 24: Common Memory Write Timing Diagram

4.3.12 I/O Input (Read) Timing Specification

Table 17: I/O Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL		35
Data Delay from Wait Rising	td(WT)	tWTHQV		0
Wait Width Time	tw(WT)	tWTLWTH		350 (3000 for *CF+*)

Note: Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0nsec, but minimum -IORD width must still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.

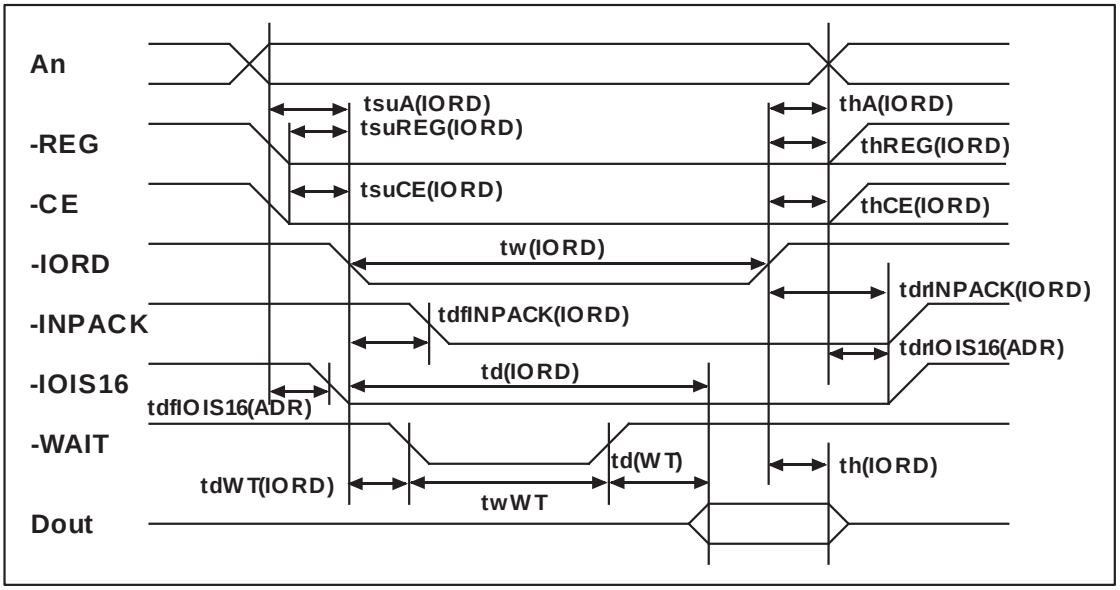


Figure 25: I/O Read Timing Diagram

4.3.13 I/O Output (Write) Timing Specification

Table 18: I/O Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL		35
IOWR high from Wait high	tdrIOWR(WT)	tWTJIWH	0	
Wait Width Time	tw(WT)	tWTLWTH		350 (3000 for *CF+*)

Note: The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0nsec, but minimum -IOWR width must still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

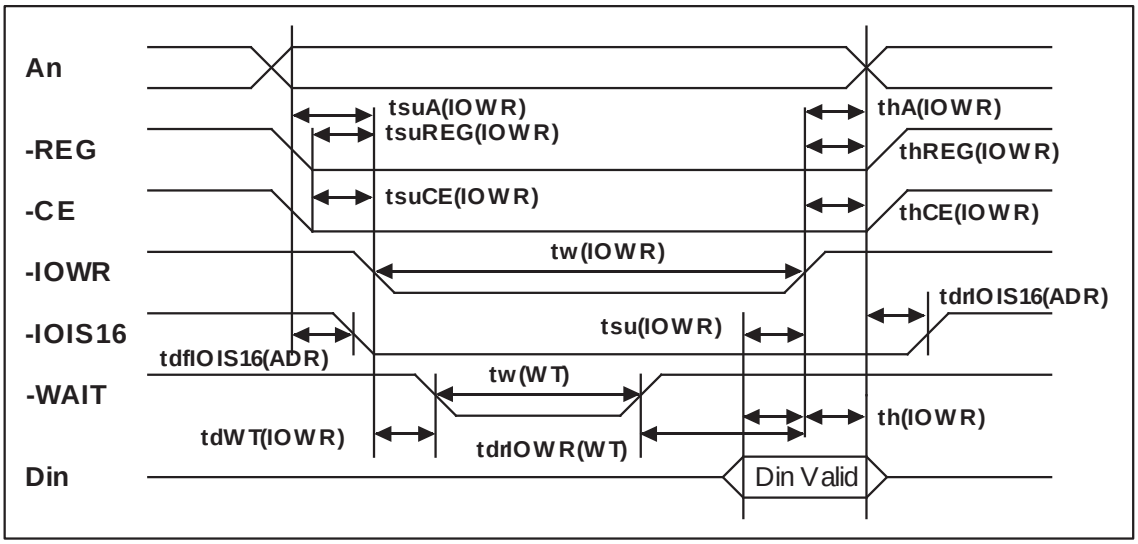


Figure 26: I/O Write Timing Diagram

4.3.14 True IDE Mode I/O Input (Read) Timing Specification

Table 19: True IDE Mode I/O Read Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

Note: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width must still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system.

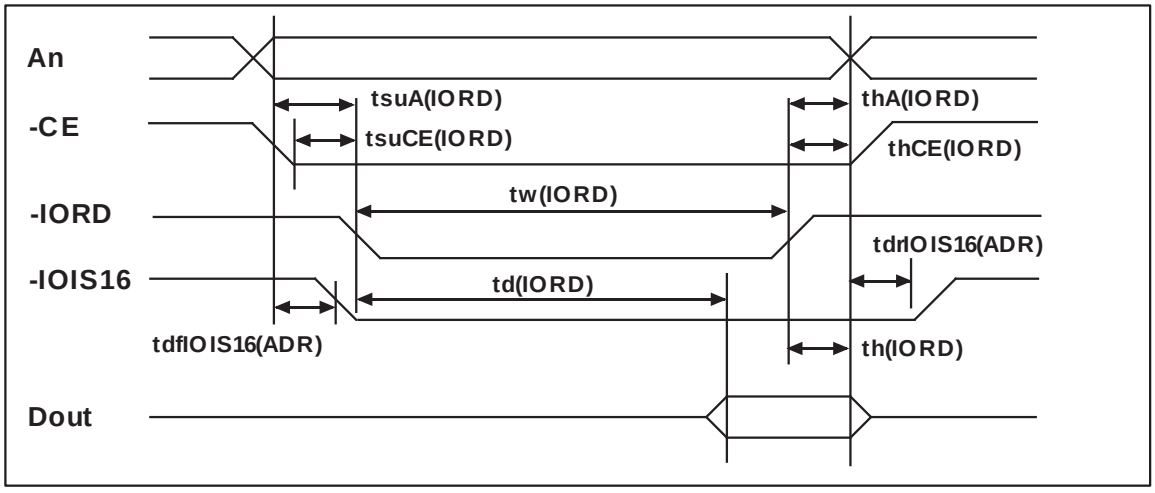


Figure 27: True IDE Mode I/O Read Timing Diagram

4.3.15 True IDE Mode I/O Output (Write) Timing Specification

Table 20: True IDE Mode I/O Write Timing

Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60	
Data Hold following IOWR	th(IOWR)	tIWHDX	30	
IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

Note: The maximum load on -IOIS16 is 1 LSTTL with 50pF total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width must still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card.

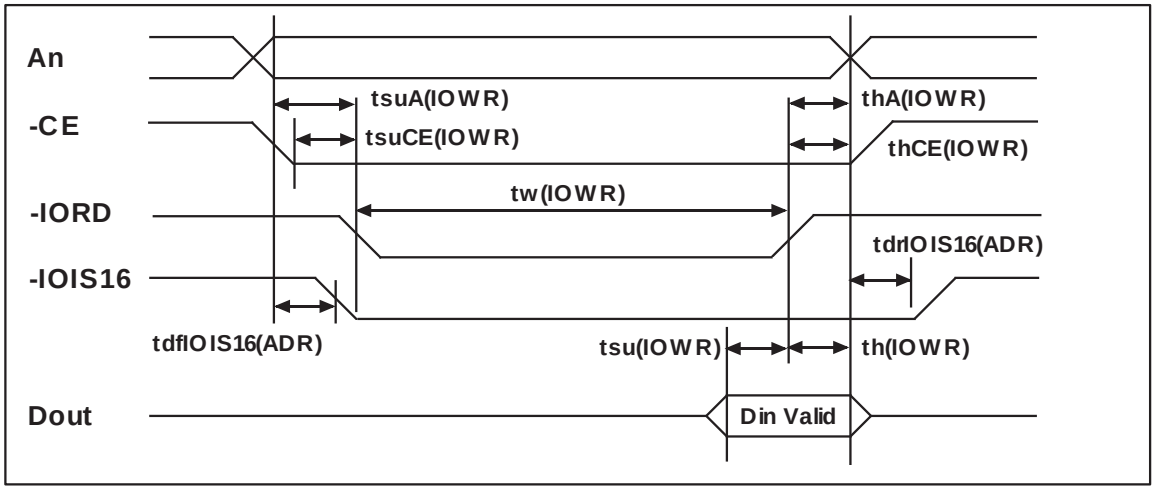


Figure 28: True IDE Mode I/O Write Timing Diagram

4.4 Card Configuration

The CompactFlash Storage Cards and CF+ Cards are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the CompactFlash Storage Card or CF+ Card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

4.4.1 Single Function CF+ Cards

Single function CF+ Cards shall have a single configuration tuple describing a single set of Function Configuration registers (see the *Metaformat Specification*). All CF+ Card configurations shall be performed using this set of Function Configuration registers.

4.4.2 Multiple Function CF+ Cards

Multiple function CF+ Cards shall have a separate set of Configuration registers for each function on the card. Multiple Function CF+ Cards shall use a combination of a global CIS common to all functions on the card and a separate function-specific CIS specific to each function on the card. The global CIS describes features that are common to all functions on the card. A CISTPL_LONGLINK_MFC tuple in the global CIS describes the location of a function-specific CIS for each function on the CF+ Card.

NOTE: a CISTPL_FUNCID with a TPLFID_FUNCTION field reset to zero (0) shall not be placed in the CIS of a Multiple Function CF+ Card. This tuple is reserved for vendor-specific multiple function CF+ Cards that do not follow the multiple function *CF+* definitions in the Standard.

Table 21: CompactFlash Storage Card Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

Table 22: CompactFlash Storage Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

Table 23: CF+ Card Register and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10-A1	A0	SELECTED SPACE
1	1	X	X	X	XXX	X	Standby
X	0	0	0	1	XXX	0	Configuration Registers Read
1	0	1	0	1	XXX	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	XXX	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	XXX	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	XXX	0	Configuration Registers Write
1	0	1	1	0	XXX	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	XXX	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	XXX	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	XXX	0	Card Information Structure Read
1	0	0	1	0	XXX	0	Invalid Access (CIS Write)
1	0	0	0	1	XXX	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	XXX	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	XXX	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	XXX	X	Invalid Access (Odd Attribute Write)

Table 24: CF+ Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10 -A5	A4	A3	A2	A1	A0	Selected Register
X	0	0	0	1	XX	0	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	XX	0	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	XX	0	0	0	1	0	Card Status Register Read
X	0	0	1	0	XX	0	0	0	1	0	Card Status Register Write
X	0	0	0	1	XX	0	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	XX	0	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	XX	0	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	XX	0	0	1	1	0	Socket and Copy Register Write
X	0	0	0	1	XX	0	1	0	0	0	Reserved
X	0	0	1	0	XX	0	1	0	1	0	I/O Base 0
X	0	0	0	1	XX	0	1	1	0	0	I/O Base 1
X	0	0	1	0	XX	0	1	1	1	0	Reserved
X	0	0	0	1	XX	1	0	0	0	0	Reserved
X	0	0	1	0	XX	1	0	0	1	0	I/O Limit
X	0	0	0	1	XX	1	0	1	0	0	Reserved

Note: For CompactFlash Storage Cards, the location of the card configuration registers should always be read from the CIS since these locations may vary in future products. For CF+ Cards, the location of the card configuration registers must always be read from the CIS. No writes should be performed to the CompactFlash Storage Card or CF+ Card attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

4.4.3 Attribute Memory Function

Attribute memory is a space where CompactFlash Storage Card and CF+ Card identification and configuration information are stored, and is limited to 8-bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash Storage Cards, the base address of the card configuration registers is 200h. For CF+ cards, the base address of the card configuration registers is determined by the Configuration tuple (CISTPL_CONFIG).

For the Attribute Memory Read function, signals -REG and -OE must be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to *Table 25* below for signal states and bus validity for the Attribute Memory function.

Table 25: Attribute Memory Function

Function Mode	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration CompactFlash Storage (8 bits)	L	H	L	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration CompactFlash Storage (8 bits)	L	H	L	L	H	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration *CF+* (8 bits)	L	H	L	X	X	L	L	H	High Z	Even Byte
Write Byte Access Configuration *CF+* (8 bits)	L	H	L	X	X	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration CompactFlash Storage (16 bits)	L	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration CompactFlash Storage (16 bits)	L	L	L	L	H	X	H	L	Don't Care	Even Byte
Read Word Access Configuration *CF+* (16 bits)	L	L	L	X	X	X	L	H	Not Valid	Even Byte
Write Word Access Configuration *CF+* (16 bits)	L	L	L	X	X	X	H	L	Don't Care	Even Byte

Note: The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

4.4.4 Configuration Option Register (Base + 00h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash Storage Card or CF+ Card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevlREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Figure 29: Configuration Option Register

SRESET - Soft Reset: setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the CompactFlash Storage Card or CF+ Card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the CompactFlash Storage Card or CF+ Card in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. For CompactFlash Storage Cards, using the PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

LevlREQ: this bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

Conf5 - Conf0 - Configuration Index: set to zero (0) by reset. It is used to select operation mode of the CompactFlash Storage Card or CF+ Card as shown below.

Note: Conf5 and Conf4 are reserved for CompactFlash Storage cards and must be written as zero (0) These bits are vendor defined for CF+ Cards.

Table 26: CompactFlash Storage Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0h-1F7h/3F6h-3F7h
0	0	0	0	1	1	I/O Mapped, 170h-177h/376h-377h

Table 27: CF+ Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	CF+ Card Mode
0	0	0	0	0	0	Memory Mapped, I/O cycles are ignored
X	X	X	X	X	X	Any non-zero value, vendor defined

On Multiple Function CF+ Cards, bits in this field enable the following functionality:

Bit 0 **Enable Function** - If this bit is reset to zero (0), the function is disabled. If this bit is set to one (1), the function is enabled.

Bit 1 **Enable Base and Limit Registers** – If this bit is reset to zero (0) and Bit 0 is set to one (1), all I/O addresses on the host system are passed to the function. If this is set to one (1) and Bit 0 is set to one (1), only I/O addresses that are qualified by the Base and Limit registers are passed to the function. If Bit 0 is reset to zero (0), this bit is undefined.

Bit 2 **Enable IREQ# Routing** – If this bit is reset to zero (0) and Bit 0 is set to one (1), this function shall not generate interrupt requests on the CF+ Card's IREQ# line. If this is set to one (1) and Bit 0 is set to one (1), this function shall generate interrupt requests on the CF+ Card's IREQ# line. If Bit 0 is reset to zero (0), this bit is undefined.

Bit 3..5 Reserved for vendor implementation.

4.4.5 Card Configuration and Status Register (Base + 02h in Attribute Memory)

The Card Configuration and Status Register contains information about the Card's condition.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	-XE	Audio	PwrDwn	Int	0
Write	0	SigChg	IOis8	-XE	Audio	PwrDwn	0	0

Figure 30: Card Configuration and Status Register

Changed: indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the CompactFlash Storage Card or CF+ Card is configured for the I/O interface.

SigChg: this bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the CompactFlash Storage Card or CF+ Card is configured for I/O.

IOis8: the host sets this bit to a one (1) if the CompactFlash Storage Card or CF+ Card is to be configured in an 8 bit I/O Mode. The CompactFlash Storage Card is always configured for both 8- and 16-bit I/O, so this bit is ignored. Some CF+ cards can be configured for either 8-bit I/O mode or 16-bit I/O mode, so CF+ cards may respond to this bit.

-XE: this bit is set and reset by the host to disable and enable Power Level 1 commands in CF+ cards. If the value is 0, Power Level 1 commands are enabled; if it is 1, Power Level 1 commands are disabled. Default value at power on or after reset is 0. The host may read the value of this bit to determine whether Power Level 1 commands are currently enabled. For CompactFlash Storage cards (which must not support Power Level 1), this bit has value 0 and is not writeable.

Audio: this bit is set and reset by the host to enable and disable audio information on SPKR# when the CF+ card is configured. This bit should always be zero for CompactFlash Storage cards.

PwrDwn: this bit indicates whether the host requests the CompactFlash Storage Card or CF+ Card to be in the power saving or active mode. When the bit is one (1), the CompactFlash Storage Card or CF+ Card enters a power down mode. When zero (0), the host is requesting the CompactFlash Storage Card or CF+ Card to enter the active mode. The PCMCIA Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The CompactFlash Storage Card automatically powers down when it is idle and powers back up when it receives a command.

Int: this bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

4.4.6 Pin Replacement Register (Base + 04h in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	Rdy/-Bsy	WProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

Figure 31: Pin Replacement Register

CRdy/-Bsy: this bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

CWProt: this bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

Rdy/-Bsy: this bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

Wprot: this bit is always zero (0) since the CompactFlash Storage Card or CF+ Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRdy/-Bsy: this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

MWProt: this bit when written acts as a mask for writing the corresponding bit CWProt.

Table 28: Pin Replacement Changed Bit/Mask Bit Values

Initial Value of (C) Status	Written by Host		Final "C" Bit	Comments
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

4.4.7 Socket and Copy Register (Base + 06h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register. This register is not required for CF+ Cards.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive #	X	X	X	X

Figure 32: Socket and Copy Register

Reserved: this bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive #: this bit indicates the drive number of the card for twin card configuration.

X: the socket number is ignored by the CompactFlash Storage Card.

4.4.8 I/O Base Register (0, 1)

The I/O Base registers are optional on single function CF+ Cards and are required on multiple function CF+ Cards. The I/O Base registers determine the base address of the I/O range used to access function-specific registers on the CF+ Card. These registers allow the CF+ Card's function-specific registers to be placed anywhere in the host system's I/O address space. The registers are written in little-endian order with the least significant byte of the base I/O address written to I/O Base 0.

The number of I/O Base Address registers implemented depends on the number of address lines the CF+ Card decodes. For example, if the function on the CF+ Card only decodes eight (8) address lines, only the first register needs to be implemented.

Offset	D7	D6	D5	D4	D3	D2	D1	D0
10	I/O Base 0							
12	I/O Base 1							

Figure 33: I/O Base Registers (0, 1)

4.4.9 I/O Limit Register

The I/O Limit register is an optional register and is only implemented on CF+ Cards that use I/O Base Address registers. If the function on the CF+ Card always uses the same number of I/O registers in all configurations, this register may be omitted (even on CF+ Cards with I/O Base Address registers).

This register specifies the number of address lines used by the function. Each bit in the register represents an I/O address line. This allows two (2) to two hundred and fifty-six (256) I/O ports to be used by a function. If a bit in the register is set to one (1), all bits of lesser significance in the register must also be set to one (1).

Offset	D7	D6	D5	D4	D3	D2	D1	D0
18	I/O Limit							

Field	Type	Description
I/O Limit	R/W	Bit-mapped register indicating the number of I/O address lines decoded by the function on the CF+ Card.

4.5 I/O Transfer Function

4.5.1 I/O Function

The I/O transfer to or from the CompactFlash Storage or CF+ Card can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Storage or CF+ Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Storage or CF+ Card, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The CompactFlash Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Storage responds. CF+ cards may or may not allow 16 bit register accesses and thus must assert IOIS16 as required.

The CompactFlash Storage and CF+ Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 29: I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

4.6 Common Memory Transfer Function

4.6.1 Common Memory Function

The Common Memory transfer to or from the CompactFlash Storage or CF+ Card can be either 8 or 16 bits.

The CompactFlash Storage Card and the CF+ Card permit both 8 and 16 bit accesses to all of its Common Memory addresses.

The CompactFlash Storage Card or the CF+ Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Table 30: Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

4.7 True IDE Mode I/O Transfer Function

4.7.1 True IDE Mode I/O Function

The CompactFlash Storage Card and CF+ Card can be configured in a True IDE Mode of operation. The CompactFlash Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. In this True IDE Mode the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode no Memory or Attribute Registers are accessible to the host. CompactFlash Storage Cards permit 8 bit data accesses if the user issues a Set Feature Command to put the device in 8 bit Mode.

Note: Removing and reinserting the CompactFlash Storage Card while the host computer's power is on will reconfigure the CompactFlash Storage Card to PC Card ATA mode from the original True IDE Mode. To configure the CompactFlash Storage Card in True IDE Mode, the 50-pin socket must be power cycled with the CompactFlash Storage Card inserted and -OE (output enable) asserted.

CF+ Card support of True IDE mode is optional.

Table 31 defines the function of the operations for the True IDE Mode.

Table 31: True IDE Mode I/O Function

Function Code	-CE2	-CE1	A0-A2	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out
Drive Address[9]	L	H	7h	L	H	High Z	Data Out

[9] Implemented for backward compatibility. User should be aware that D7 may conflict with floppy implementation. Avoid use in new designs.

5 Metaformat

5.1 Metaformat Overview

The goal of the Metaformat is to describe the requirements and capabilities of the CompactFlash Storage Card and CF+ Card as thoroughly as possible. This includes describing the power requirements, IO and memory requirements, information about the manufacturer and details about the services provided.

The Metaformat is a hierarchy of layers. Each layer has a number, which increases as the level of abstraction gets higher. Included are layers to describe the data recording format and data organization, for memory and ATA cards that wish to adhere to the CFA/PCMCIA specification. Below the Metaformat is the physical layer, the electrical and physical characteristics of CF+ Cards. The CF+ Metaformat conforms directly to the PCMCIA Metaformat Specification, March 1997. Refer to that document for a detailed description of the Metaformat.

5.2 Metaformat Requirements

The CF+ Cards have the following Card Information Structure (CIS) requirements:

- All CF+ Cards have a CIS that describes the functionality and characteristics of the card
- The CIS of a CF+ Card shall be readable whenever the card is powered, the card is asserting READY and the card has been reset by the host after power-up in accordance with the CompactFlash Standard. This includes after the CF+ Card is configured and when the PwrDwn bit is set in the Card Configuration and Status Register. (See the *Electrical Specification*, section 4.)
- All CF+ Cards shall provide at least the mandatory Tuples as described in the PCMCIA Metaformat Specification, March 1997, Tuple Summary Table.
- All linear memory CF+ Cards shall describe how they are partitioned, even if the entire CF+ Card is used as a single partition.

6 Software Interface

6.1 CF-ATA Drive Register Set Definition and Protocol

The CompactFlash Storage Card can be configured as a high performance I/O device through:

a) Standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary); 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).

b) Any system decoded 16 byte I/O block using any available IRQ.

c) Memory space.

The communication to or from the CompactFlash Storage Card is done using the Task File registers which provide all the necessary registers for control and status information. The PCMCIA interface connects peripherals to the host using four register mapping methods. *Table 32* is a detailed description of these methods:

Table 32: I/O Configurations

Standard Configurations			
Config Index	**I/O or Memory**	**Address**	**Description**
0	Memory	0h-Fh, 400h-7FFh	Memory Mapped
1	I/O	XX0h-XXFh	I/O Mapped 16 Contiguous Registers
2	I/O	1F0h-1F7h, 3F6h-3F7h	Primary I/O Mapped
3	I/O	170h-177h, 376h-377h	Secondary I/O Mapped

Note: Refer to Section 4.3.5 for Twin Card implementation.

6.1.1 I/O Primary and Secondary Address Configurations

Table 33: Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data	1, 2
0	1F(17)h	0	0	0	1	Error Register	Features	1, 2
0	1F(17)h	0	0	1	0	Sector Count	Sector Count	
0	1F(17)h	0	0	1	1	Sector No.	Sector No.	
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)h	0	1	1	1	Status	Command	
0	3F(37)h	0	1	1	0	Alt Status	Device Control	
0	3F(37)h	0	1	1	1	Drive Address	Reserved	

Note: 1) Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers which lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

2) A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

6.1.2 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CompactFlash Storage Card, the registers are accessed in the block of I/O space decoded by the system as follows:

Table 34: Contiguous I/O Decoding

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card /Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

Note: 1) Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2) Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.

Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.

Repeated byte accesses to register 8 or 0 will access consecutive (even than odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3) Address lines which are not indicated are ignored by the CompactFlash Storage Card for accessing all the registers in this table.

6.1.3 Memory Mapped Addressing

When the CompactFlash Storage Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as follows:

Table 35: Memory Mapped Decoding

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1, 2
1	0	X	0	0	0	1	1	Error	Features	1, 2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card /Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

Note: 1) Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2) Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.

Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.

Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3) Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 Kbyte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.

Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the CompactFlash Storage Card.

A word access to address at offset 8 will provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high-order byte of the data bus.

6.1.4 True IDE Mode Addressing

When the CompactFlash Storage Card or CF+ Card is configured in the True IDE Mode, the I/O decoding is as follows:

Table 36: True IDE Mode I/O Decoding

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0	Note
1	0	0	0	0	RD Data	WR Data	
1	0	0	0	1	Error Register	Features	
1	0	0	1	0	Sector Count	Sector Count	
1	0	0	1	1	Sector No.	Sector No.	
1	0	1	0	0	Cylinder Low	Cylinder Low	
1	0	1	0	1	Cylinder High	Cylinder High	
1	0	1	1	0	Select Card/Head	Select Card/Head	
1	0	1	1	1	Status	Command	
0	1	1	1	0	Alt Status	Device Control	
0	1	1	1	1	Drive Address	Reserved	

6.1.5 CF-ATA Registers

The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the "task file."

Note: In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted) and an I/O cycle is being performed.

6.1.5.1 Data Register (Address - 1F0h[170h];Offset 0,8,9)

The Data Register is a 16-bit register, and it is used to transfer data blocks between the CompactFlash Storage Card data buffer and the Host. This register overlaps the Error Register. The table below describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

Note: Because of the overlapped registers, access to the 1F1h, 171h or offset 1 are not defined for word (-CE2 = 0 and -CE1 = 0) operations. These accesses are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed by the socket.

Table 37: Data Register Access

Data Register	CE2-	CE1-	A0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	D15-D0
Even Data Register	1	0	0	0,8	D7-D0
Odd Data Register	1	0	1	9	D7-D0
Odd Data Register	0	1	X	8,9	D15-D8
Error / Feature Register	1	0	1	1, Dh	D7-D0
Error / Feature Register	0	1	X	1	D15-D8
Error / Feature Register	0	0	X	Dh	D15-D8

6.1.5.2 Error Register (Address - 1F1h[171h]; Offset 1, 0Dh Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Figure 34: Error Register

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -CE2 low and -CE1 high.

Bit 7 (BBK): this bit is set when a Bad Block is detected.

Bit 6 (UNC): this bit is set when an Uncorrectable Error is encountered.

Bit 5: this bit is 0.

Bit 4 (IDNF): the requested sector ID is in error or cannot be found.

Bit 3: this bit is 0.

Bit 2 (Abort) This bit is set if the command has been aborted because of a CompactFlash Storage Card status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

Bit 1 This bit is 0.

Bit 0 (AMNF) This bit is set in case of a general error.

6.1.5.3 Feature Register (Address - 1F1h[171h]; Offset 1, 0Dh Write Only)

This register provides information regarding features of the CompactFlash Storage Card that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high.

6.1.5.4 Sector Count Register (Address - 1F2h[172h]; Offset 2)

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Storage Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

6.1.5.5 Sector Number (LBA 7-0) Register (Address - 1F3h[173h]; Offset 3)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash Storage Card data access for the subsequent command.

6.1.5.6 Cylinder Low (LBA 15-8) Register (Address - 1F4h[174h]; Offset 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

6.1.5.7 Cylinder High (LBA 23-16) Register (Address - 1F5h[175h]; Offset 5)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

6.1.5.8 Drive/Head (LBA 27-24) Register (Address 1F6h[176h]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Figure 35: Drive/Head Register

Bit 7: this bit is set to 1.

Bit 6: LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

LBA7-LBA0: Sector Number Register D7-D0.

LBA15-LBA8: Cylinder Low Register D7-D0.

LBA23-LBA16: Cylinder High Register D7-D0.

LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5: this bit is set to 1.

Bit 4 (DRV): DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. The CompactFlash Storage Card is set to be Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.

Bit 3 (HS3): when operating in the Cylinder , Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2): when operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1): when operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0): when operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

6.1.5.9 Status & Alternate Status Registers (Address 1F7h[177h]&3F6h[376h]; Offsets 7 & Eh)

These registers return the CompactFlash Storage Card status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Figure 36: Status & Alternate Status Register

Bit 7 (BUSY): the busy bit is set when the CompactFlash Storage Card has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY): RDY indicates whether the device is capable of performing CompactFlash Storage Card operations. This bit is cleared at power up and remains cleared until the CompactFlash Storage Card is ready to accept a command.

Bit 5 (DWF): This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC): This bit is set when the CompactFlash Storage Card is ready.

Bit 3 (DRQ): The Data Request is set when the CompactFlash Storage Card requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR): This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX): This bit is always set to 0.

Bit 0 (ERR): This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is recommended that media access commands (such as Read Sectors and Write Sectors) that end with an error condition should have the address of the first sector in error in the command block registers.

6.1.5.10 Device Control Register (Address - 3F6h[376h]; Offset Eh)

This register is used to control the CompactFlash Storage Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Figure 37: Device Control Register

Bit 7: this bit is an X (don't care).

Bit 6: this bit is an X (don't care).

Bit 5: this bit is an X (don't care).

Bit 4: this bit is an X (don't care).

Bit 3: this bit is ignored by the CompactFlash Storage Card.

Bit 2 (SW Rst): this bit is set to 1 in order to force the CompactFlash Storage Card to perform an AT Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration Registers (4.3.2 to 4.3.5) as a hardware Reset does. The Card remains in Reset until this bit is reset to '0.'

Bit 1 (-IEn): the Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the CompactFlash Storage Card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.

Bit 0: this bit is ignored by the CompactFlash Storage Card.

6.1.5.11 Card (Drive) Address Register (Address 3F7h[377h]; Offset Fh)

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Figure 38: Card (Drive) Address Register

Bit 7: this bit is unknown.

Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the CompactFlash Storage Card. Following are some possible solutions to this problem for the PCMCIA implementation:

1) Locate the CompactFlash Storage Card at a non-conflicting address, i.e. Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses.

2) Do not install a Floppy and a CompactFlash Storage Card in the system at the same time.

3) Implement a socket adapter which can be programmed to (conditionally) tri-state D7 of I/0 address 3F7h/377h when a CompactFlash Storage Card is installed and conversely to tri-state D6-D0 of I/O address 3F7h/377h when a floppy controller is installed.

4) Do not use the CompactFlash Storage Card's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0h-1F7h, 3F6h (or 170h-177h, 176h) to the CompactFlash Storage Card or b) if provided use an additional Primary / Secondary configuration in the CompactFlash Storage Card which does not respond to accesses to I/O locations 3F7h and 377h. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG): this bit is 0 when a write operation is in progress, otherwise, it is 1.

Bit 5 (-HS3): this bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (-HS2): this bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (-HS1): this bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (-HS0): this bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (-nDS1): this bit is 0 when drive 1 is active and selected.

Bit 0 (-nDS0): this bit is 0 when the drive 0 is active and selected.

6.2 CF-ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the CompactFlash Storage Cards. Commands are issued to the CompactFlash Storage Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 5-6) of command acceptance, all dependent on the host not issuing commands unless the CompactFlash Storage Card is not busy (BSY=0). All commands listed in this specification shall be implemented. Commands can be implemented as “no operation” to meet this requirement.

- Upon receipt of a Class 1 command, the CompactFlash Storage Card sets BSY within 400nsec.
- Upon receipt of a Class 2 command, the CompactFlash Storage Card sets BSY within 400nsec, sets up the sector buffer for a write operation, sets DRQ within 700µsec, and clears BSY within 400nsec of setting DRQ.
- Upon receipt of a Class 3 command, the CompactFlash Storage Card sets BSY within 400nsec, sets up the sector buffer for a write operation, sets DRQ within 20msec (assuming no re-assignments), and clears BSY within 400nsec of setting DRQ.

6.2.1 CF-ATA Command Set

Table 38 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 38: CF-ATA Command Set

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Drive Diagnostic	90h	-	-	-	-	D	-
1	Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Drive	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense	03h	-	-	-	-	D	-
1	Security Disable Password	F6h	-	-	-	-	D	-
1	Security Erase Prepare	F3h	-	-	-	-	D	-
1	Security Erase Unit	F4h	-	-	-	-	D	-
1	Security Freeze Lock	F5h	-	-	-	-	D	-
1	Security Set Password	F1h	-	-	-	-	D	-
1	Security Unlock	F2h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Stand By	E2h or 96h	-	-	-	-	D	-
1	Stand By Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

Definitions:

- FR = Features Register
- SC = Sector Count Register
- SN = Sector Number Register
- CY = Cylinder Registers
- DH = Card/Drive/Head Register
- LBA = Logical Block Address Mode Supported (see command descriptions for use).
- Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash Storage Card and head parameters are used; D - only the CompactFlash Storage Card parameter is valid and not the head parameter.

6.2.1.1 Check Power Mode - 98h or E5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98h or E5h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 39: Check Power Mode

This command checks the power mode.

If the CompactFlash Storage Card is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt.

If the CompactFlash Storage Card is in Idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

6.2.1.2 Execute Drive Diagnostic - 90h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 40: Execute Drive Diagnostic

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card.

If in PCMCIA configuration this command runs only on the CompactFlash Storage Card which is addressed by the Drive/Head register when the diagnostic command is issued. This is because PCMCIA card interface does not allows for direct inter-drive communication (such as the ATA PDIAG and DASP signals). If in True IDE Mode the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices.

The Diagnostic codes shown in *Table 39* are returned in the Error Register at the end of the command.

Table 39: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

6.2.1.3 Erase Sector(s) - C0h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 41: Erase Sector

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

6.2.1.4 Format Track - 50h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Count (LBA mode only)							
Feature (1)	X							

Figure 42: Format Track

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

6.2.1.5 Identify Drive – Ech

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 43: Identify Drive

The Identify Drive command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in *Table 40*. All reserved bits or words are zero. *Table 40* is the definition for each field in the Identify Drive Information.

Table 40: Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the CompactFlash Storage Card
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	XXXXh	2	Number of unformatted bytes per track
5	XXXXh	2	Number of unformatted bytes per sector
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	XXXXh	2	Vendor Unique
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	XXXXh	2	Buffer type
21	XXXXh	2	Buffer size in 512 byte increments
22	0004h	2	# of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	XXXXh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Double Word not supported
49	XX00h	2	Capabilities
50	0000h	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
51	0X00h	2	PIO data transfer cycle timing mode
52	0000h	2	DMA data transfer cycle timing mode
53	0001h	2	Translation parameters are valid
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	010Xh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62-127	0000h	138	Reserved
128	XXXXh	2	Security status
129-159	0000h	64	Vendor unique bytes
160	XXXXh	2	Power requirement description
161-255	0000h	170	Reserved

6.2.1.5.1 General Configuration

This field indicates that the device is a CompactFlash Storage Card.

6.2.1.5.2 Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

6.2.1.5.3 Default Number of Heads

This field contains the number of translated heads in the default translation mode.

6.2.1.5.4 Number of Unformatted Bytes per Track

This field contains the number of unformatted bytes per translated track in the default translation mode.

6.2.1.5.5 Number of Unformatted Bytes per Sector

This field contains the number of unformatted bytes per sector in the default translation mode.

6.2.1.5.6 Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

6.2.1.5.7 Number of Sectors per Card

This field contains the number of sectors per CompactFlash Storage Card. This double word value is also the first invalid address in LBA translation mode.

6.2.1.5.8 Memory Card Serial Number

The contents of this field are right justified and padded with spaces (20h).

6.2.1.5.9 Buffer Type

This field defines the buffer capability:

0000h: not specified.

0001h: a single ported single sector buffer which is not capable of simultaneous data transfers to or from the host and the device.

0002h: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the CompactFlash Storage Card.

0003h: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the CompactFlash Storage Card with a read caching capability.

6.2.1.5.10 Buffer Size

This field defines the buffer capacity in 512 byte increments.

6.2.1.5.11 ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands.

6.2.1.5.12 Firmware Revision

This field contains the revision of the firmware for this product.

6.2.1.5.13 Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

6.2.1.5.14 Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

6.2.1.5.15 Double Word Support

This field indicates this product will not support double word transfers.

6.2.1.5.16 Capabilities

Bit 13: Standby Timer
if set to 1, indicates that the Standby timer is supported as defined by the IDLE command
if set to 0, indicates that the Standby timer operation is defined by the vendor.

Bit 11: IORDY Support
if set to 1, indicates that this device supports IORDY operation.
if set to 0, indicates that this device may support IORDY operation.

Bit 9: LBA support
CompactFlash Storage Cards support LBA mode addressing.

Bit 8: DMA Support
if set to 1, Read DMA and Write DMA commands are supported.
This bit should be set to 0. DMA mode is not supported.

6.2.1.5.17 PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer.

6.2.1.5.18 DMA Data Transfer Cycle Timing Mode

This field defines the mode for DMA data transfer.

6.2.1.5.19 Translation Parameters Valid

This field contains the value 0001h indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors.

6.2.1.5.20 Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

6.2.1.5.21 Current Capacity

This field contains the product of the current cylinders times heads times sectors.

6.2.1.5.22 Multiple Sector Setting

This field contains a validity flag in the odd byte and the current number of sectors that can be transferred per interrupt for R/W Multiple in the even byte. The odd byte is always 01h which indicates that the even byte is always valid.

The even byte value depends on the value set by the Set Multiple command. The even byte of this word by default contains a 00h which indicates that R/W Multiple commands are not valid.

6.2.1.5.23 Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the CompactFlash Storage Card in LBA mode only.

6.2.1.5.24 Security Status

Bit 8: Security Level
if set to 1, indicates that security mode is enabled and the security level is maximum.
if set to 0 and security mode is enabled, indicates that the security level is high.

Bit 4: Expire
If set to 1, indicates that the security count has expired and SECURITY UNLOCK and SECURITY ERASE UNIT are command aborted until a power-on reset or hard reset.

Bit 3: Freeze
if set to 1, indicates that the security is Frozen.

Bit 2: Lock
if set to 1, indicates that the security is locked.

Bit 1: Enable/Disable
if set to 1, indicates that the security is enabled.
If set to 0, indicates that the security is disabled.

Bit 0: Capability
if set to 1, indicates that CompactFlash Storage Card supports security mode feature set.
if set to 0, indicates that CompactFlash Storage Card does not support security mode feature set.

6.2.1.5.25 Power Requirement Description

Bit 15: VLD
if set to 1, indicates that this word contains a valid power requirement description.
if set to 0, indicates that this word does not contain a power requirement description.

Bit 14: RSV
This bit is reserved and must be 0.

Bit 13: -XP
if set to 1, indicates that the CompactFlash Storage Card does not have Power Level 1 commands.
if set to 0, indicates that the CompactFlash Storage Card has Power Level 1 commands

Bit 12: -XE
if set to 1, indicates that Power Level 1 commands are disabled..
if set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current
This field contains the CompactFlash Storage Card's maximum current in mA.

6.2.1.6 Idle - 97h or E3h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97h or E3h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

Figure 44: Idle

This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

6.2.1.7 Idle Immediate - 95h or E1h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95h or E1h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 45: Idle Immediate

This command causes the CompactFlash Storage Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

6.2.1.8 Initialize Drive Parameters - 91h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	91h							
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Number of Sectors							
Feature (1)	X							

Figure 46: Initialize Drive Parameters

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command.

6.2.1.9 Read Buffer - E4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E4h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 47: Read Buffer

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

6.2.1.10 Read Multiple - C4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 48: Read Multiple

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = (sector count) - modulo (block count).

If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

6.2.1.11 Read Long Sector - 22h or 23h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	22h or 23h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 49: Read Long Sector

The Read Long command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes. During a Read Long command, the CompactFlash Storage Card does not check the ECC bytes to determine if there has been a data error. Only single sector read long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

6.2.1.12 Read Sector(s) - 20h or 21h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20h or 21h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 50: Read Sector(s)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the CompactFlash Storage Card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

6.2.1.13 Read Verify Sector(s) - 40h or 41h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40h or 41h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 51: Read Verify Sector(s)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY.

When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

6.2.1.14 Recalibrate - 1Xh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1Xh							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 52: Recalibrate

This command is effectively a NOP command to the CompactFlash Storage Card and is provided for compatibility purposes.

6.2.1.15 Request Sense - 03h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03h							
C/D/H (6)	1	X	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 53: Request Sense

This command requests extended error information for the previous command. *Table 41* defines the valid extended error codes for the CompactFlash Storage Card Series product. The extended error code is returned to the host in the Error Register.

Table 41: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed
22h	Power Level 1 Disabled

6.2.1.16 Security Disable Password - F6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F6h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 54: Security Disable Password

This command requests a transfer of a single sector of data from the host. *Table 42* defines the content of this sector of information. If the password selected by word 0 matches the password previously saved by the device, the device disables the lock mode. This command does not change the Master password that may be reactivated later by setting a User password.

Table 42: Security Password Data Content

Word	Content
0	Control word Bit 0: identifier 0=compare User password 1=compare Master password Bit 1-15: Reserved
1-16	Password (32 bytes)
17-256	Reserved

6.2.1.17 Security Erase Prepare - F3h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F3h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 55: Security Erase Prepare

This command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental erase of the CompactFlash Storage Card.

6.2.1.18 Security Erase Unit - F4h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F4h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 56: Security Erase Unit

This command requests transfer of a single sector of data from the host. *Table 42* defines the content of this sector of information. If the password does not match the password previously saved by the CompactFlash Storage Card, the CompactFlash Storage Card rejects the command with command aborted. The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the CompactFlash Storage Card receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the CompactFlash Storage Card command aborts the SECURITY ERASE UNIT command.

6.2.1.19 Security Freeze Lock - F5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 57: Security Freeze Lock

The SECURITY FREEZE LOCK command sets the CompactFlash Storage Card to Frozen mode. After command completion any other commands that update the CompactFlash Storage Card Lock mode are rejected. Frozen mode is disabled by power off or hardware reset. If SECURITY FREEZE LOCK is issued when the CompactFlash Storage Card is in Frozen mode, the command executes and the CompactFlash Storage Card remains in Frozen mode. After command completion the Sector Count Register shall be set to 0.

Commands disabled by SECURITY FREEZE LOCK are:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT

If security mode feature set is not supported, this command shall be handled as WEAR LEVEL command.

6.2.1.20 Security Set Password - F1h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F1h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 58: Security Set Password

This command requests a transfer of a single sector of data from the host. *Table 43* defines the content of the sector of information. The data transferred controls the function of this command. *Table 44* defines the interaction of the identifier and security level bits.

Table 43: SECURITY SET PASSWORD Data Content

Word	Content
0	Control word Bit 0: Identifier 0=set User password 1=set Master password Bits 1-7: Reserved Bit 8: Security level 0=High 1=Maximum Bits 9-15: Reserved
1-16	Password (32 bytes)
17-255	Reserved

Table 44: Identifier and Security Level Bit Interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The CompactFlash Storage Card shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new user password. The lock mode shall be enabled from the next power-on reset or hardware reset. The CompactFlash Storage Card shall then be unlocked by only the User password. The Master password previously set is still stored in the CompactFlash Storage Card shall not be used to unlock the CompactFlash Storage Card.
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed.

6.2.1.21 Security Unlock - F2h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F2h							
C/D/H (6)	1	LBA	1	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 59: Security Unlock

This command requests transfer of a single sector of data from the host. *Table 42* defines the content of this sector of information. If the identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. if the device is in maximum security level then the unlock shall be rejected. If the identifier bit is set to user then the device compares the supplied password with the stored User password. If the password compare fails then the device returns command aborted to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when SECURITY UNLOCK is issued and the device is locked. When this counter reaches zero then SECURITY UNLOCK and SECURITY ERASE UNIT commands are command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

6.2.1.22 Seek - 7Xh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7Xh							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 60: Seek

This command is effectively a NOP command to the CompactFlash Storage Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

6.2.1.23 Set Features – Efh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

Figure 61: Set Features

This command is used by the host to establish or select certain features. Table 45 defines all features that are supported.

Table 45: Feature Supported

Feature	Operation
01h	Enable 8-bit data transfers.
0Ah	Enable Power Level 1 commands
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset.
69h	NOP - Accepted for backward compatibility.
81h	Disable 8-bit data transfer.
8Ah	Disable Power Level 1 commands
96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
BBh	4 bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers will occur on the low order D7D0 data bus and the IOIS16 signal will not be asserted for data register accesses.

Features 0Ah and 8Ah are used to enable and disable Power Level 1 commands. Feature 0Ah is the default feature for the CompactFlash Storage Card with extended power.

Features 55h and BBh are the default features for the CompactFlash Storage Card; thus, the host does not have to issue this command with these features unless it is necessary for compatibility reasons.

Feature code 9Ah enables the host to configure the card to best meet the host system's power requirements. The host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register is set to 6, the card would be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the host with the range of values supported by the card. The minimum value is set in the Cylinder

Low register, and the maximum value is set in the Cylinder Hi register. The default value, after a power on reset, is to operate at the highest performance and therefore the highest current mode. The card will accept values outside this programmable range, but will operate either at the lowest power or highest performance as appropriate.

Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) Defaults will be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.

6.2.1.24 Set Multiple Mode - C6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 62: Set Multiple Mode

This command enables the CompactFlash Storage Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the CompactFlash Storage Card sets BSY to 1 and checks the Sector Count Register.

If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write Multiple disabled.

6.2.1.25 Set Sleep Mode- 99h or E6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99h or E6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 63: Set Sleep Mode

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5 msec) is different from the ATA Specification.

6.2.1.26 Standby - 96h or E2h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96h or E2h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 64: Standby

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.2.1.27 Standby Immediate - 94h or E0h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94h or E0h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 65: Standby Immediate

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.2.1.28 Translate Sector - 87h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 66: Translate Sector

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector. *Table 46* represents the information in the buffer. Please note that this command is unique to the CompactFlash Storage Card.

Table 46: Translate Sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04h-06h	LBA MSB (04) - LSB (06)
07h-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h – 17h	Reserved
18h-1Ah	Hot Count MSB (18) - LSB (1A) [1]
1Bh-1FFh	Reserved

Note 1: A value of 0 indicates Hot Count is not supported.

6.2.1.29 Wear Level - F5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	F5h							
C/D/H (6)	X	X	X	Drive	Flag			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Completion Status							
Feature (1)	X							

Figure 67: Wear Level

For the CompactFlash Storage Cards that do not support security mode feature set, this command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a 00h indicating Wear Level is not needed. If the CompactFlash Storage Card supports security mode feature set, this command shall be handled as Security Freeze Lock.

6.2.1.30 Write Buffer - E8h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 68: Write Buffer

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

6.2.1.31 Write Long Sector - 32h or 33h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	32h or 33h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

Figure 69: Write Long Sector

This command is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes. Only single sector Write Long operations are supported. The transfer consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC transferred in byte mode. Because of the unique nature of the solid-state CompactFlash Storage Card, the four bytes of ECC transferred by the host may be used by the CompactFlash Storage Card. The CompactFlash Storage Card may discard these four bytes and write the sector with valid ECC data. This command has the same protocol as the Write Sector(s) command. Use of this command is not recommended.

6.2.1.32 Write Multiple Command - C5h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5h							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 70: Write Multiple Command

Note: The current revision of the CompactFlash Storage Card only supports a block count of 1 as indicated in the Identify Drive Command information. This command is provided for compatibility with future products which may support a larger block count.

This command is similar to the Write Sectors command. The CompactFlash Storage Card sets BSY within 400 nsec of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.

When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = sector count (modulo sector/block).

If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.

Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command, e.g., each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.

6.2.1.33 Write Multiple without Erase – CDh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDh							
C/D/H (6)	X	LBA	X	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 71: Write Multiple without Erase

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued.

6.2.1.34 Write Sector(s) - 30h or 31h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30h or 31h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 72: Write Sector(s)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash Storage Card sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

6.2.1.35 Write Sector(s) without Erase - 38h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38h							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 73: Write Sector(s) without Erase

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased with the Erase Sector(s) command, a normal write sector operation will occur.

6.2.1.36 Write Verify - 3Ch

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3Ch							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Figure 74: Write Verify

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command.

6.2.2 Error Posting

Table 47 summarizes the valid status and error value for all the CF-ATA Command set.

Table 47: Error and Status Register

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Check Power Mode				V		V	V	V		V
Execute Drive Diagnostic[1]						V		V		V
Erase Sector(s)	V		V	V	V	V	V	V		V
Format Track			V	V	V	V	V	V		V
Identify Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Drive Parameters						V		V		V
Read Buffer				V		V	V	V		V
Read Multiple	V	V	V	V	V	V	V	V	V	V
Read Long Sector	V		V	V	V	V	V	V		V
Read Sector(s)	V	V	V	V	V	V	V	V	V	V
Read Verify Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request Sense				V		V		V		V
Security Disable Password				V		V	V	V		V
Security Erase Prepare				V		V	V	V		V
Security Erase Unit				V		V	V	V		V
Security Freeze Lock				V		V	V	V		V
Security Set Password				V		V	V	V		V
Security Unlock				V		V	V	V		V
Seek			V	V		V	V	V		V
Set Features				V		V	V	V		V
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Stand By				V		V	V	V		V
Stand By Immediate				V		V	V	V		V
Translate Sector	V		V	V	V	V	V	V		V
Wear Level	V	V	V	V	V	V	V	V		V
Write Buffer				V		V	V	V		V
Write Long Sector	V		V	V	V	V	V	V		V
Write Multiple	V		V	V	V	V	V	V		V

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Write Multiple w/o Erase	V		V	V	V	V	V	V		V
Write Sector(s)	V		V	V	V	V	V	V		V
Write Sector(s) w/o Erase	V		V	V	V	V	V	V		V
Write Verify	V		V	V	V	V	V	V		V
Invalid Command Code				V		V	V	V		V

V = valid on this command

[1] See Table 5-7.

6.2.3 Security Mode Feature Set

The Security Mode feature set allows a host to implement a security password system to prevent unauthorized access to the CompactFlash Storage Card. A device that implements the Security Mode feature set shall implement the following minimum set of commands:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT
- SECURITY FREEZE LOCK
- SECURITY DISABLE PASSWORD

Support of the Security Mode feature set is indicated in IDENTIFY DEVICE word 128.

6.2.3.1 Security Mode Default Setting

The Master password shall be set to a vendor specific value during manufacturing and the Lock mode disabled. The system manufacturer/dealer may set a new Master password using the SECURITY SET PASSWORD command, without enabling or disabling the Lock mode.

6.2.3.2 Initial Setting of the User Password

When a User password is set, the device shall automatically enter Lock mode the next time the device is powered-on or after a hardware reset.

6.2.3.3 Security Mode Operation From Power-On or Hardware Reset

When Lock is enabled, the device rejects media access commands until a SECURITY UNLOCK command is successfully completed.

6.2.3.4 Frozen Mode

The SECURITY FREEZE LOCK command places the device in Frozen mode. This prevents accidental or malicious password activation or setting. *Table 48* lists the commands that the device shall execute when in Frozen mode. The device shall exit Frozen mode on power off. All devices that support the Security Mode feature set should be issued a SECURITY FREEZE LOCK command during system initialization.

6.2.3.5 User Password Lost

If the User password does not match and High level security is set, the device shall not allow the user to access data. The device shall be unlocked using the Master password. If the User password is lost and Maximum security level is set, data access shall not be allowed. However, the SECURITY ERASE UNIT command shall unlock the device and shall erase all user data if the Master password matches.

6.2.3.6 Attempt Limit for SECURITY UNLOCK Command

The device shall have an attempt limit counter. The purpose of this counter is to defeat repeated trial attacks. After each failed User or Master password SECURITY UNLOCK command, the counter is decremented. When the counter value reaches zero the EXPIRE bit (bit 4) of word 128 in the IDENTIFY DEVICE information is set, and the SECURITY UNLOCK and SECURITY UNIT ERASE commands are command aborted until the device is powered off or hardware reset. The EXPIRE bit shall be cleared to zero after power on or hardware reset. The counter shall be set to five after a power on or hardware reset.

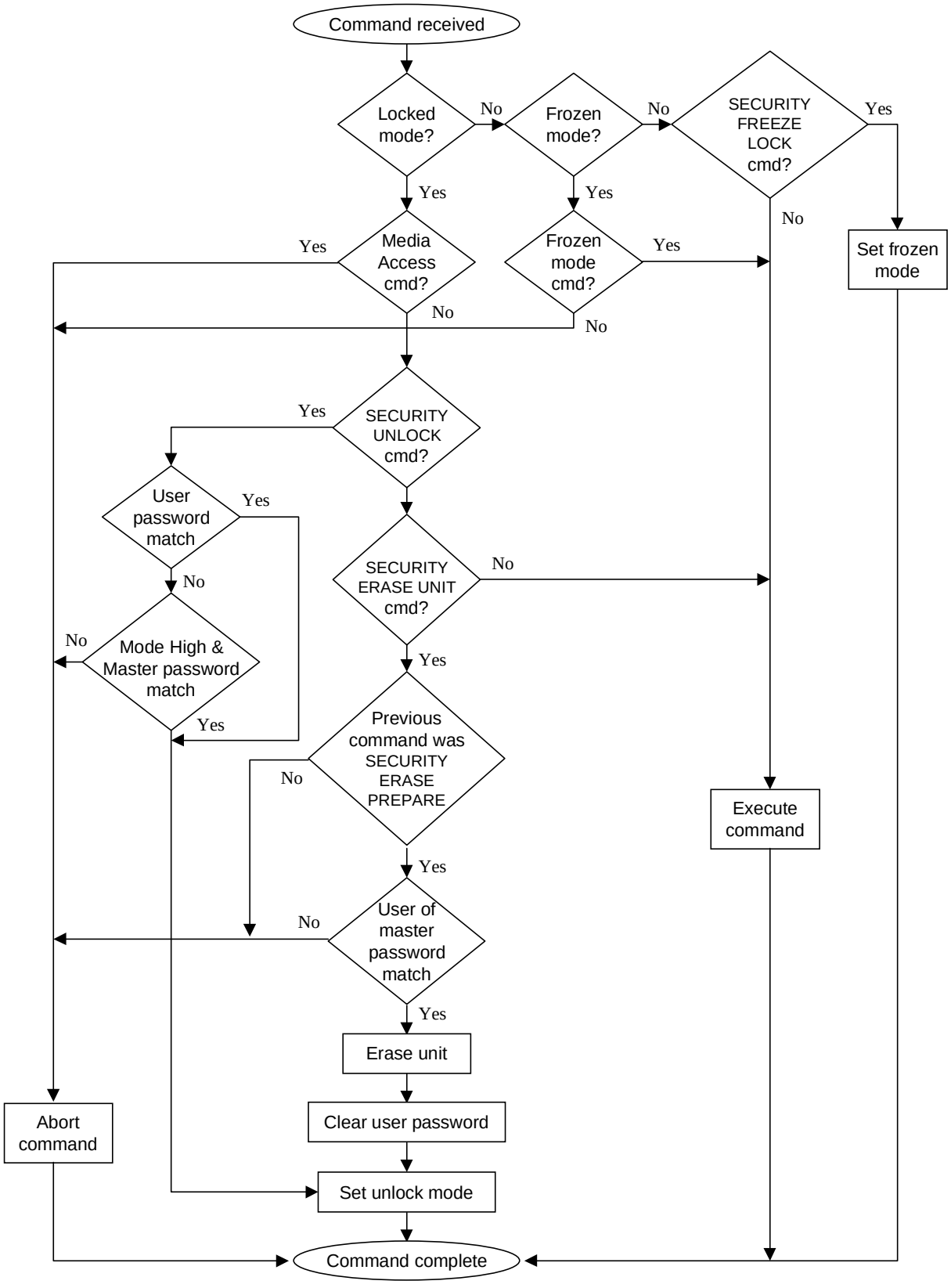


Figure 75: Security Mode Flow

Table 48: Security Mode Command Actions

Command	Locked Mode	Unlocked Mode	Frozen Mode
Check Power Mode	O	O	O
Execute Drive Diagnostic	O	O	O
Erase Sector(s)	X	O	O
Format Track	X	O	O
Identify Drive	O	O	O
Idle	O	O	O
Idle Immediate	O	O	O
Initialize Drive Parameters	O	O	O
Read Buffer	O	O	O
Read Multiple	X	O	O
Read Long Sector	X	O	O
Read Sector(s)	X	O	O
Read Verify Sectors	X	O	O
Recalibrate	O	O	O
Request Sense	O	O	O
Security Disable Password	X	O	X
Security Erase Prepare	O	O	O
Security Erase Unit	O	O	X
Security Freeze Lock	X	O	O
Security Set Password	X	O	X
Security Unlock	O	O	X
Seek	O	O	O
Set Features	O	O	O
Set Multiple Mode	O	O	O
Set Sleep Mode	O	O	O
Stand By	O	O	O
Stand By Immediate	O	O	O
Translate Sector	O	O	O
Wear Level	O	O	O
Write Buffer	O	O	O
Write Long Sector	X	O	O
Write Multiple	X	O	O
Write Multiple w/o Erase	X	O	O
Write Sector(s)	X	O	O
Write Sector(s) w/o Erase	X	O	O
Write Verify	X	O	O

7 CompactFlash Adapter

7.1 Overview

CompactFlash and CF+ Type 1 products can be used with a PCMCIA Type II passive adapter. This adapter converts the Type 1 CompactFlash Storage Card or CF+ Card into a Type II PCMCIA PC card. CF adapters must physically and electrically conform to the PCMCIA PC Card Standard.

NOTE: At this time there is no specification for a CF Type II to PCMCIA Type II adapter. Various proposals have been put forth to the CFA and are under review. Contact the CFA for information regarding the status of the official CF Type II to PCMCIA Type II adapter.

7.2 CompactFlash Adapter Specifications

Refer to *Table 49* and *Figure 76* for the CompactFlash Adapter physical specifications.

Table 49: CompactFlash Adapter Physical Specifications

Length:	85.6 ± 0.20 mm (3.370 ±.008 in)
Width:	54.0 ± 0.10 mm (2.126 ± .004 in)
Thickness:	5.0 mm max. (0.1968 in)

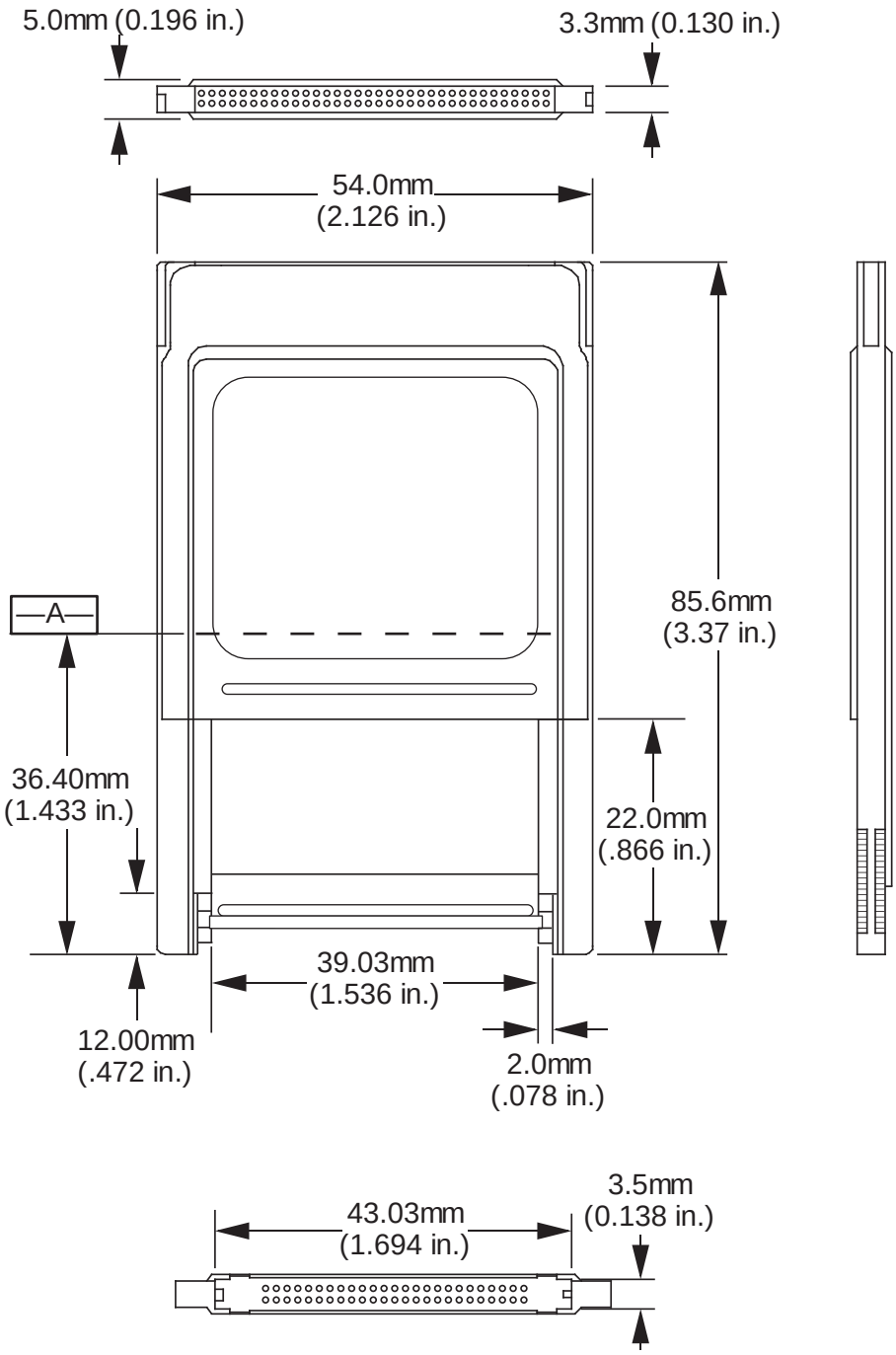


Figure 76: Type 1 CompactFlash Adapter

7.3 Electrical Differences Between the Type 1 CompactFlash Storage/CF+ Card and the Type 1 CompactFlash Adapter

The CompactFlash Storage Card and the CompactFlash CF+ Card are electrically compatible with the Type II CompactFlash Adapter. Both conform to the PCMCIA PC Card Standard. CompactFlash products use a 50-pin connector and CompactFlash Adapters use a 68-pin connector. Both connectors use less than 50 signals. *Table 50* shows the pinout differences between the CompactFlash Storage/CF+ Card and the CompactFlash Adapter.

Table 50: Pinout Differences Between CF Storage Card and CF Adapter

	CF Adapter	CF Storage/ CF+ Card		CF Adapter	CF Storage/ CF+ Card
Pin 1	GND	GND	Pin 35	GND	-IOWR
Pin 2	D03	D03	Pin 36	-CD1	-WE
Pin 3	D04	D04	Pin 37	D11	-RDY/-BSY/-IREQ
Pin 4	D05	D05	Pin 38	D12	VCC
Pin 5	D06	D06	Pin 39	D13	-CSEL
Pin 6	D07	D07	Pin 40	D14	-VS2
Pin 7	-CE1	-CE1	Pin 41	D15	RESET
Pin 8	A10	A10	Pin 42	-CE2	-WAIT
Pin 9	-OE	-OE	Pin 43	-VS1	-INPACK
Pin 10	A11	A09	Pin 44	-IORD	-REG
Pin 11	A09	A08	Pin 45	-IOWR	BVD2
Pin 12	A08	A07	Pin 46	A17	BVD1
Pin 13	A13	VCC	Pin 47	A18	D08
Pin 14	A14	A06	Pin 48	A19	D09
Pin 15	-WE	A05	Pin 49	A20	D10
Pin 16	-RDY/-BSY/-IREQ	A04	Pin 50	A21	GND
Pin 17	VCC	A03	Pin 51	VCC	
Pin 18	VPP1	A02	Pin 52	VPP2	
Pin 19	A16	A01	Pin 53	A22	
Pin 20	A15	A00	Pin 54	A23	
Pin 21	A12	D00	Pin 55	A24	
Pin 22	A07	D01	Pin 56	A25	
Pin 23	A06	D02	Pin 57	-VS2	
Pin 24	A05	WP\-IOIS16	Pin 58	RESET	
Pin 25	A04	-CD2	Pin 59	-WAIT	
Pin 26	A03	-CD1	Pin 60	-INPACK	
Pin 27	A02	D11	Pin 61	-REG	
Pin 28	A01	D12	Pin 62	BVD2	
Pin 29	A00	D13	Pin 63	-STSCHG	
Pin 30	D00	D14	Pin 64	D08	

	CF Adapter	CF Storage/ CF+ Card		CF Adapter	CF Storage/ CF+ Card
Pin 31	D01	D15	Pin 65	D09	
Pin 32	D02	-CE2	Pin 66	D10	
Pin 33	WP/-IOIS16	-VS1	Pin 67	-CD2	
Pin 34	GND	-IORD	Pin 68	GND	

7.3.1 CompactFlash Adapter Card Resistance

When measured between the solder lead pad on the 50 position straddle mount header and the solder lead pad on the 68 position receptacle, there should be 150 milliohms maximum bulk resistance per circuit.

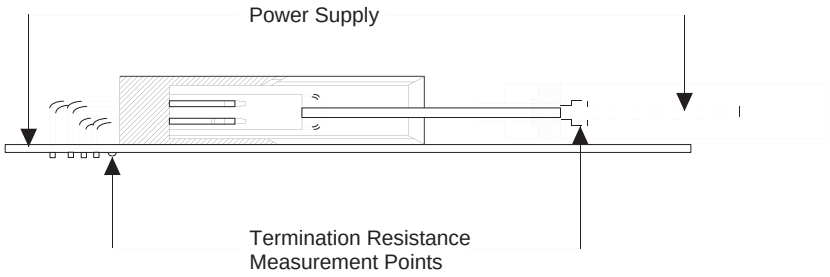


Figure 77: Termination Resistance Measurement Points

Table 51: Termination Resistance Procedure

Test Description	Requirement	Procedure
Termination Resistance	Initial: Signal, 260 milliohms maximum. Ground, 100 milliohms maximum. • R 20 milliohms maximum.	Subject samples to 50 mV maximum open circuit at 100 mA maximum.

7.4 CF Adapter Design Considerations

It is recommended that the 68-pin PCMCIA to 50-pin CF adapter board be constructed with a multi-layer board having a ground plane along with ground traces between signals on the top and bottom of this board for electrical cross-talk isolation.

8 Appendix

8.1 Differences between CF/CF+ and PCMCIA, and between CF-ATA and PC Card-ATA/True IDE

This section details differences between CF/CF+ vs. PC Card, CF-ATA vs. PC Card ATA and between CF-ATA vs. True IDE.

8.1.1 CF/CF+ Electrical Differences

8.1.1.1 TTL Compatibility

CF is not TTL compatible, it is a purely CMOS interface. Refer to *Section 4.2* of this specification.

8.1.1.2 Pull Up Resistor Input Leakage Current

The minimum pull up resistor input leakage is 50k ohms rather than the 10k ohms stated in the PCMCIA specification.

8.1.1.3 Wait Width Time

The Wait Width Time for CompactFlash Storage Cards is 350 ns and is 3μs for CF+ Cards, rather than 12 μs as stated in the PCMCIA specification.

8.1.2 ATA Functional Differences

8.1.2.1 Set Features Codes not Supported

The following Set Features codes are specified in, but not implemented in CF-ATA:

- 03h, Set Transfer Mode
- 44h, Vendor unique ECC length
- AAh, Enable Read Look Ahead

8.1.2.2 Additional Set Features Codes in CF-ATA

The following Set Features codes are not PC Card ATA or True IDE, but provide additional functionality in CF-ATA.

- 69h, Accepted for backward compatibility
- 96h, Accepted for backward compatibility
- 97h, Accepted for backward compatibility
- 9Ah, Set the host current source capability

8.1.2.3 Additional Commands in CF-ATA

The following commands are not standard PC Card ATA commands, but provide additional functionality in CF-ATA.

The command codes for the commands below are defined as vendor unique in PC Card ATA/True IDE.

- C0h, Erase Sectors
- 87h, Translate Sector
- F5h, Wear Level

The command codes for the commands below are defined as reserved in PC Card ATA/True IDE:

- 03h, Request Sense
- 38h, Write Without Erase
- CDh, Write Multiple Without Erase

8.1.2.4 Idle Timer

The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in PC Card ATA/True IDE.

8.1.2.5 Recovery from Sleep Mode

For CF Storage devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.

8.2 Differences Between CompactFlash Storage Cards and CF+ Cards

CompactFlash and other Data Storage Cards must have their Configuration Registers at offset 200h. On non-data storage CF+ Cards the location of the Configuration Registers is determined by parsing the CIS (Tuples).

CompactFlash and other Data Storage Cards need to support a Maximum Wait Width pulse of 350 ns, whereas non-data storage CF+ Cards only need to support a 3us pulse.

CompactFlash and other Data Storage Cards must support all three access modes, memory, I/O and True IDE, whereas non-data storage CF+ Cards only need to support memory and I/O access (True IDE mode is optional).

Any card that uses Power Level 1, either via the configuration registers or ATA commands, is considered a CF+ card.

9 Revision History

Revision Level	Changes
1.0	Initial Release.
1.1	General editorial changes; addition of connector drawings.
1.2	Correction of millimeter to inch conversions on drawings; general editorial changes.
1.3	Added CF Type II drawing and dimensions; added CF adapter bulk resistance measurement instructions; added datum A at card socket to drawings.
1.4	Added CF+ Specifications. Added updated ATA Command set. Changed name to CF+ & CompactFlash, incorporated comments regarding Power and True IDE mode. Editorial changes. Added CompactFlash vs. CF+ Appendix. Added power measurement schematic. Added note regarding CF Type II to PCMCIA adapter. Added CF Type II host connector. Updated Figure 13, “Surface Mount Right Angle CF/CF+ Type I Card Slot Header” drawing.